LeCroy

CAMAC TO GPIB
INTERFACE
MODEL 8901A

Revised
January, 1986

WARRANTY

LECROY RESEARCH SYSTEMS CORP. warrants each instrument it manufacturers to be free from defects in material and workmanship under normal use and service for the period of 1-year from date of purchase. Custom monolithics and hybrids sold separately and all spare or replacement parts and repairs are warranted for 90 days. This warranty extends only to the original purchaser and shall not apply to fuses, disposable batteries, or any product or parts which have been subject to misuse, neglect, accident or abnormal conditions of operations.

In the event of failure of a product covered by this warranty, LeCroy will repair and calibrate an instrument returned to the factory or an authorized service facility within one year of the original purchase; provided the warrantor's examination discloses to its satisfaction that the product was defective. The warrantor may, at its option, replace the product in lieu of repair. Wtih regard to any instrument returned within one year of the original purchase, said repairs or replacement will be made without charge. If the failure has been caused by misuse, neglect, accident, or abnormal conditions or operations, repairs will be billed at a nominal cost. In such cases, an estimate will be submitted before work is started, if requested.

The foregoing warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy Research Systems Corp., shall not be liable for any special, incidental, or consequential damages, whether in contract, tort or otherwise.

IF ANY FAILURE OCCURS, notify LeCroy Research Systems Corp., or the nearest service facility, giving full details of the difficulty, and include the Model number, serial number, and FAN (Final Assembly Number) or ECO (Engineering Change Order) number. On receipt of this information, service data or shipping instructions will be forwarded to you. On receipt of the shipping instructions, forward the instrument, transportation prepaid. A Return Authorization Number will be given as part of shipping instructions. Marking this RA number on the outside of the package will insure that it goes directly to the proper department within LeCroy. Repairs will be made at the service facility and the instrument returned transportation prepaid.

ALL SHIPMENTS OF LeCROY INSTRUMENTS FOR REPAIR OR ADJUSTMENT should be made via Air Freight or "Best Way" prepaid. the instrument should be shipped in the original packing carton; or if it is not available, use any suitable container that is rigid and of adequate size. If a substitute container is used, the instrument should be wrapped in paper and surrounded with at least four inches of excelsior or similar shock-absorbing material.

IN EVENT OF DAMAGE IN SHIPMENT to original purchaser the instrument should be thoroughly inspected immediately upon original delivery to purchaser. All material in the container should be checked against the enclosed Packing List. The manufacturer will not be responsibe for shortages against the packing sheet unless notified immediately. If the instrument is damaged in any way, a claim should be filed with the carrier immediately. (To obtain a quotation to repair shipment damage, contat the LeCroy factory or the nearest service facility).

DOCUMENTATION DISCREPANCIES OR OMISSIONS. LeCroy Corporation is committed to providing unique, reliable, state-of-the-art instrumentation in the field of high-speed data acquisition and processing. Because of this commitment, the Engineering Department at LeCroy is continually refining and improving the performance of products. While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purposes of pulse shape, timing, offset, etc., and, only rarely include minor logic changes. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

ANY APPLICATION OR USE QUESTIONS, which will enhance your use of this instrument will be happily answered by a member of our Engineering Services Department, telephone 914-425-2000 or your local distributor. You may address any correspondence to:

LeCroy Corporation, 700 S. Main Street,
Spring Valley, New York 10977, ATTN: Customer Service Dept. or
LeCroy Corporation, 14800 Central S.E.,
Albuquerque, New Mexico 87123
LeCroy Corporation, 1816 Holmes Street, Bldg. E
Livermore, California 94550

European Customers can contact:

LeCroy Research Systems Ltd.
Elms Court
Botley
Oxford OX2 9LP England

LeCroy Research Systems SA
101 Route Du Nant-D'Avril
1217 Meyrin 1-Geneve
Switzerland

LeCroy Research Sys. S.a.r.l.
Avenue Du Parana
Z.A. De Courtaboeuf
F-91940 Les Ulis, France

LeCroy Research Systems GmbH
Werderstrasse 48
Postfach 10 37 67
6900 Heidelberg
West Germany

A T T E N T I O N

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LISTS, AND ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF UNIT TO AVOID DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

A T T E N T I O N

TABLE OF CONTENTS

		Page
1.	Technical Data Sheet	
2.	Operation	2-1
	2.1 Introduction	2-1
	2.2 Setup Commands	2-1
	2.2.1 Transfer Mode Commands	2-1
	2.2.2 Service Requests Response Commands	2-2
	2.3 Programming CAMAC Modules	2-3
	2.3.1 Commands Common to all Instruments	2-3
	2.3.2 Commands to an Individual Instrument	2-4
	2.4 Hardware Configuration	2-4
	2.5 Programming Example	2-5
3.	Theory of Operation	3-1
	3.1 General	3-1
	3.2 GPIB Command Decoder	3-2
	3.3 Acceptor Handshake	3-2
	3.4 Listen Mode	3-2
	3.5 Global CAMAC Commands	3-2
	3.6 F,A,N CAMAC Commands	3-2
	3.7 8901A Commands	3-2
	3.8 Serial Poll Mode	3-2
	3.9 Talk Mode	3-3
	3.10 Source Handshake	3-3
	3.11 CAMAC Cycle Timing	3-3
	3.12 Read Data	3-3
	3.13 X and Q Response	3-4
	3.14 LAM Lines	3-4
	3.15 SRQ Generation	3-4
Block Diagram		
Appendix A		
	Description of CAMAC	
	Application Note 2015	
	Schematics	

LeCroy

CAMAC TO GPIB INTERFACE*
Model 8901A

- **Allows GPIB users access to the wide range of inexpensive instrumentation available from LeCroy and other CAMAC manufacturers**
- **Converts a CAMAC mainframe with up to 23 individual instruments into standard GPIB Listener/Talker**
- **Block Transfer Mode allows transfer of all data from a CAMAC module upon receipt of a single talk command at rates up to 500 kilobytes/sec**
- **The 8901A is fully compatible with LeCroy's Series 6900 WAVEFORM-CATALYST Software for the IBM PC**

Simple program instructions via the GPIB to registers in the Model 8901A select an individual instrument module within the CAMAC mainframe, select any subaddress within that module, and establish the function (read, write, control). This allows the user to handle the entire CAMAC mainframe of up to 23 individual instrument modules in the same manner as any ordinary single device connected to the IEEE-488 bus. It is possible to interconnect up to 15 different CAMAC mainframes in this way.

The 8901A can be programmed to do a block transfer of all data within a CAMAC module to a GPIB Listener without additional intermediate commands. In this mode, the 8901A will alternately transfer one, two or three 8-bit bytes (as programmed) as fast as the Listener can accept them (at rates approaching 500 kilobytes/sec) and then initiate a new CAMAC acquisition cycle.

As the list of computer, programmable calculator and intelligent terminal manufacturers offering the GPIB grows, so do the inherent advantages of uniting the GPIB and CAMAC concepts. The combination enhances the flexibility of both standards, decreases per-channel cost and retains most performance characteristics of each.

The cost of a CAMAC mainframe (housing, power supply and internal digital bus) approximately equals the usual packaging cost of a single stand-alone instrument. As a result, the economic advantage of buying one GPIB interface and CAMAC crate for up to 23 individual instruments is substantial.

*CAMAC Computer Automated Measurement and Control (IEEE Standard 583-1975)

*GPIB General Purpose Interface Bus (IEEE Standard 488-1978)

Preliminary - June 1985

Corporate Headquarters: 700 South Main Street, Spring Valley, NY 10977, USA. Tel: (914) 425-2000, TWX: 710-577-2832

European Headquarters: Route du Nant-d'Avril 101 CH-1217 Meyrin 1-Geneva, Switzerland. Tel: (022) 82 33 55, Telex: 28230

SPECIFICATIONS

CAMAC TO GPIB INTERFACE

LOADING THE INTERNAL REGISTERS

Registers in the 8901A interface are sequentially loaded with data after it has been commanded to enter the Listen mode by the GPIB System Controller. These registers store all the information necessary (F, A, N. W, C, Z, I) to generate standard CAMAC cycles.

The first byte received by the interface after it has entered the Listen mode contains either the CAMAC Function (F Code) or control information. The second and sequential bytes accept, respectively, the CAMAC subaddress (A Code), station number (N Code) and three bytes of data for the CAMAC write lines.

Once these registers have been loaded, the information will be retained until modified or power is turned off. The GPIB system controller must issue a Listen command in order to initiate this loading procedure. The loading process can be terminated after any number of bytes have been transferred by issuing a Talk, Listen, Unlisten or IFC command.

INITIATING CAMAC CYCLES

A CAMAC cycle is executed every time the 8901A is commanded to enter the Talk mode and a Service Request is not pending. At the completion of the CAMAC cycle a DAV (Data Valid) will be asserted. Every time a byte is accepted a new byte is made available. When no more data is available, the 8901A asserts End of Identity (EOI).

CLEAR, INITIALIZE, AND INHIBIT

The 8901A can be programmed to generate clear (C), initialize (Z), or inhibit (I) signals on the dataway when a CAMAC cycle is executed. The C and Z registers are cleared after the completion of the next CAMAC cycle. The inhibit register will remain set until it is programmed off.

BLOCK TRANSFER MODE

The 8901A can be programmed to do a high speed block transfer of 8-, 16- or 24-bit words from CAMAC modules with read and increment capability. Following module addressing and the appropriate control byte, a Talk command will start the 8901A to read one, two, or three bytes of data and automatically initiate another CAMAC cycle. Approximatley 2 µsec later (a programmable 40 µsec delay can be used for slow modules) new data is available to be read. CAMAC cycles will continue to be exectued until a Q=0 (end of memory) condition causes the 8901A to stop executing CAMAC cycles and exit the transfer mode.

SERVICE REQUESTS

The 8901A will issue a Service Request when a LAM is set by a CAMAC module, or when a CAMAC cycle is executed and a Q=0 or X=0 response is detected.

SERIAL POLL

When the 8901A is polled, it sends up to five status bytes to the controller, terminating the Request after the controller reads the status byte. For a LAM-generated Service Request the LAM must be cleared or disabled before the poll is taken, or else another service request will immediately be issued.

FRONT PANEL LED'S

TALK:	Indicates when 8901A is a Talker.
LISTEN:	Indicates when 8901A is a Listener.
SRQ ENABLE:	Indicates when 8901A is enabled to carry out Service Requests.
X RESPONSE:	Indicates a valid command was accepted in the mainframe.
Q RESPONSE:	Indicates a valid data transfer or valid test within the mainframe.
LOOK-AT-ME:	Indicates when any CAMAC module sets "LAM" (a Service Request).
INHIBIT:	Indicates when CAMAC dataway is inhibited.

GPIB ADDRESS SWITCH

Sets the GPIB Address of the 8901A.

GENERAL

The 8901A resides in the two slots furthest right in a CAMAC mainframe and generates all CAMAC dataway signals in response to commands from a GPIB controller. A standard GPIB connector on the front panel permits easy interconnection to any GPIB system. This allows any GPIB controller to program settings, read from or write to any standard CAMAC module.

Packaging is in conformance with CAMAC standard, RF shielded #2 module.

Power Required is 1.2 A at +6 V

SPECIFICATIONS SUBJECT TO CHANGE

2. OPERATION

2.1 Introduction

For those unfamiliar with CAMAC, it is an international standard for modularized instrumentation as defined by the ESONE Committee and the IEEE (Standard #583). Its function is to provide a means by which a wide range of modular instruments can be powered in a multi-receptacle crate and interfaced to a controller. This controller may be interfaced to a computer. In this way, additions to a data acquisition and control system may be made by plugging in additional modules and making suitable software changes. The LeCroy Model 8901A CAMAC to GPIB (IEEE 488) interface allows the benefits of CAMAC system configuration to be incorporated with GPIB computer controllers. For additional information on the IEEE 583 CAMAC standard, See Appendix A.

The Model 8901A is a direct replacement for both the LeCroy Model 8901 and 8901/100 (Mod 100) and will work with LeCroy 6900 series CATALYST software. In addition to all of the 8901-8901/100 features, the "A" version includes the generation of the GPIB EOI signal at the end of valid data, a jumper to select the order in which data bytes are sent to the GPIB controller, and a "slow" block mode transfer for instruments that cannot be read out at full CAMAC speed.

The GPIB controller may send the 8901A two types of commands. The first type, setup commands, program the 8901A, while the second type, CAMAC commands, is used by the 8901A to program the operation of instruments in the mainframe.

2.2 Setup Commands

The setup commands are used to program the 8901A for the desired transfer mode, SRQ (service request) response and can generate the CAMAC clear, initialize, and inhibit signals. All of these commands are single bytes; that is, the 8901A must first be addressed to Listen, followed by the command byte.

2.2.1 Transfer Mode Commands

By sending the appropriate command (see Table 1), the 8901A can be programmed to return 8, 16, or 24-bit data words, whenever it executes a CAMAC cycle. In the case of multiple byte transfers, the least significant byte is sent first (if the byte jumpers are set to normal - see Section 2.4 for more details). A CAMAC cycle is executed every time the 8901A is addressed to Talk by the GPIB controller. If a "block mode" read command had been sent, the 8901A will automatically initiate another CAMAC cycle when the GPIB controller has finished reading the current data word. CAMAC cycles will continue to be executed until Q = 0 or the GPIB controller terminates the transfer. There are two block modes in the 8901A. The first one, "block read" is provided for modules which cannot read out at full CAMAC speed (1 MHz). In this mode, a 35 usec delay (plus

GPIB overhead) is added between each CAMAC cycle to slow down the transfer rate. The other mode, "high speed block read" runs as fast as the data is read out over the GPIB, up to 2 usec per cycle.

In normal mode, after the 1, 2, or 3 data bytes have been read, a status byte is sent containing the X response (least significant bit) and the Q response (bit 2) along with the GPIB EOI status line asserted to indicate that this is the end of the data to be transferred. When block mode transfers are terminated normally (data read until Q=0) two additional bytes are sent to the GPIB controller. The first one is the status byte followed by a zero byte and EOI.

Note that in block mode transfers, since the 8901A is initiating the CAMAC cycles, if the GPIB controller terminates the transfer before Q=0, one additional cycle will be executed and the data will be left in the 8901A's registers. To access this data it is necessary to send the CAMAC command F(0), A(0), and N(24) (see next section) and then read out the data word. At the end of the block transfer, the 8901A is set to the corresponding normal transfer mode.

	Normal Transfer	Block Read	High Speed Block Read
8-bit read	97 (61)	121 (79)	105 (69)
16-bit read	98 (62)	122 (7A)	106 (6A)
24-bit read	100 (64)	124 (7C)	108 (6C)

Table 1 - Transfer Mode Commands
Single byte commands - values specified in decimal
with hex value given in ()

2.2.2 Service Request Response Commands

A service request (SRQ) is a mechanism by which a GPIB compatible instrument can tell a computer that a particular condition exists, without the computer having to read a byte of information. There are three conditions occurring on the CAMAC bus which can cause the Model 8901A to issue a service request to the GPIB controller: When a LAM is set, and when Q and/or X indicate that invalid data/commands occurred during a transfer. Table 2 below lists the commands to send to the 8901A to set it up to generate a SRQ on the proper condition(s).

The GPIB controller must perform a serial poll of all devices after receiving a service request. When the 8901A is polled, it sends up to 5 bytes of information to the GPIB controller. The first byte is a status byte which contains the current state of X and Q in bits 1 (LSB) and 2 respectively and bit 7 indicating whether or not the currently addressed 8901A was the device which requested service. If

bit 7 is equal to one, the 8901A generated the request. The next four bytes indicate the state of the LAM lines. They are encoded as follows:

LAM for slots 1 through 6 are in byte 2 (LAM 1 is LSB)
LAM for slots 7 through 12 are in byte 3
LAM for slots 13 through 18 are in byte 4
LAM for slots 19 through 23 are in byte 5

A service request by the 8901A will be cleared after the controller reads the status byte. However, if the request was caused by a LAM, a service request will immediately be issued again unless SRQ on LAM is disabled in the 8901A or the LAM is cleared in the instrument(s) asserting it. It is important to note that the 8901A cannot execute any CAMAC commands while any service request is pending.

Disable all SRQ's	64	(40)
Enable SRQ on occurrence of LAM	65	(41)
Enable SRQ on occurrence of Q=0	66	(42)
Enable SRQ on occurrence of X=0	68	(44)
Enable SRQ on occurrence of LAM or Q=0	67	(43)
Enable SRQ on occurrence of LAM or X=0	69	(45)
Enable SRQ on occurrence of Q=0 or X=0	70	(46)
Enable SRQ on occurrence of LAM, Q=0, or X=0	71	(47)

Table 2 - Service Request Response Commands
NOTE: All of these commands deassert inhibit

Single byte commands - values specified in decimal
with hex value given in ()

2.3 Programming CAMAC Instruments

2.3.1. Commands Common to All Instruments

The 8901A can be programmed to generate clear (C), initialize (Z), or inhibit (I) signals on the Dataway when a CAMAC cycle is executed. As described earlier, these commands operate on all instruments in the mainframe without any further addressing. The clear and initialize signals will be turned on only during the first CAMAC cycle executed after the 8901A received that command. The inhibit line will remain asserted until the 8901A is programmed to deassert it. Caution - changing the inhibit line will affect the state of the service request response programming. Table 3 lists the 8901A commands to perform these functions.

Send initialize (Z)	33	(21)
Send clear (C)	34	(22)
Send clear and initialize	35	(23)
Assert inhibit (I)	72	(48)

Deassert inhibit (also disables SRQ's) 64 (40)

Table 3 - CAMAC Commands
(single byte commands - values specified in decimal)

2.3.2 Commands to an Individual Instrument

To send a CAMAC command to a particular instrument the GPIB controller must address the 8901A to Listen and load it with the desired command information. If the first byte received by the interface after entering Listen mode is a valid CAMAC function (F) code, (0 to 31) the 8901A assumes that it is being sent a command sequence. The second byte expected is the CAMAC subaddress (A) code. This is followed by the CAMAC station number (N) code and up to three bytes of data (least significant byte first). Once the command is sent to the 8901A the information will be retained until modified or the power is turned off. The GPIB system computer may terminate the command loading procedure after any number of bytes have been sent. In other words, if the only difference between the last CAMAC command and the next one to be sent is the F code, it is not necessary to send a new A, N, etc.

After loading the 8901A with the desired command, a CAMAC cycle must be executed (by addressing the 8901A to Talk) to send the command to the particular instrument (see Transfer Mode Commands for more details).

2.4 Hardware Configuration

GPIB Address

Each device connected to the GPIB must have a unique address which the system controller uses to communicate with it. The address of the Model 8901A is set by a DIP switch located under the GPIB connector on the front panel. The switches are labeled A0,A1,A2,A3,A4 (representing values of 1,2,4,8,16 respectively). Valid GPIB address are 0 to 31. Figure 6.1 shows an example address setting.

address 5:

```
GPIB ADDRESS
   X     X   X  X  0
X     X           1
A0 A1 A2 A3 A4  -
```

where X indicates switch depressed

Figure 6.1 GPIB Address Switch Settings

Byte Order Jumpers

On the side panel of the Model 8901A are two pair of jumpers labeled "NORMAL" and "REVERSE". These jumpers determine the order in which the data bytes are read out. When the jumpers are set to normal, the least significant byte of data is read out first in multibyte transfers. When in the reverse byte position, a 16-bit word is read out, most significant byte first, followed by the least significant byte. If 24-bit transfer is selected, the order is middle byte, least significant byte and then most significant byte. It is recommended that the reverse byte option only be used when the computer expects the MSB before the LSB in a 16-bit word. Caution - this jumper only controls the byte order for reading out of the 8901A. It does not effect the "write" data.

2.5 Programming Example

The following example illustrates the use of most of the 8901A commands. The procedure uses a typical sequence of commands to control a LeCroy Model TR8837F Transient Recorder, as shown below. For purposes of this example, assume that the Model 8901A is at GPIB address 1 and the Model TR8837F is in slot 3.

initialize the instruments upon power on

enable LAM

initiate sampling

wait for trigger

enable TR8837 for reading

read data out in high speed mode

read acquisition parameters

The implementation of this sequence (from the GPIB system controller) is given below. The following notation is used:

OUT x,y,...	indicates a transfer from the GPIB controller to the 8901A. It includes addressing the 8901A to Listen, sending the data byte(s) to it, and then sending the GPIB Unlisten command.
IN b1,...bn,r	indicates a n+1 byte transfer from the 8901A to the GPIB controller (b1 ... bn are data bytes, r is the CAMAC response byte with bits X and Q). It includes addressing

the appropriate 8901A to Talk, reading the data byte(s) into the computer, and then sending the GPIB Untalk.

TALK

indicates sending out the GPIB Talk address to the specific 8901A. This is used to execute a CAMAC cycle when no data is to be returned. The "IN" command may be substituted if desired (e.g., to allow monitoring the CAMAC response bits X and Q).

	GPIB bus transfers (bytes in decimal)
INITIALIZE THE INSTRUMENTS	
Initialize the crate by sending CAMAC Z	OUT 33
Execute CAMAC cycle by addressing 8901A to Talk	TALK
Program instrument's parameters by sending F(16), A(0), N(3), d1, d2 (d1, d2 are the parameter settings - see TR8837F manual for details)	OUT 16,0,3,d1,d2
Program 8901A to return 8 bits of data and the CAMAC response byte	OUT 97
Execute CAMAC cycle and get CAMAC response	IN b1, r
ENABLE LAM	
Program 8901A to set SRQ on LAM	OUT 65
Enable TR8837F to generate LAM by sending F(26) (note that since the A and N have not changed it is not necessary to resend them)	OUT 26
Execute CAMAC cycle by addressing 8901A to Talk	TALK
INITIATE SAMPLING	
Initiate sampling in the TR8837F with a F(9), A(0),N(3)	OUT 9,0,3
Execute CAMAC cycle by addressing 8901A to Talk	TALK
WAIT FOR TRIGGER	
At this point, the TR8837F is waiting for a trigger (either external or from an F(25) sent to it). After the trigger occurs and the module is finished acquiring data, it will generate a service request.	
Perform a serial poll to determine which instrument set LAM (assuming there is more than one).	
Disable the 8901A from generating another SRQ	OUT 64
Send the GPIB serial poll enable command	SPE
Read in the 5 status bytes	IN r,L1,L2,L3,L4
Send the GPIB serial poll disable command	SPD

ENABLE TR8837F FOR READING	
Clear LAM in TR8837F with F(10),A(0),N(3)	OUT 10,0,3
Execute CAMAC cycle by addressing 8901A to Talk	TALK 1
Enable read mode in the TR8837F with an F(17), A(0),N(3)	OUT 17,0,3
Execute CAMAC cycle by addressing 8901A to Talk	TALK
READ DATA	
Set 8901A up for a high speed block read of 8-bit data words	OUT 105
Send F(2) to TR8837F - command to read data	OUT 2,0,3
Execute a CAMAC cycle and read all of the data out (at end of data, module sets Q to 0, the 8901A then sends the response byte followed by a 0 with the GPIB EOI bit set	IN b1,...,bn,r,0
READ ACQUISITION PARAMETERS	
Program the 8901A for a 16-bit data word	OUT 98
Tell the TR8837F to send its parameters (F(0),A(0),N(0))	OUT 0,0,3
Execute CAMAC cycle and get 2 bytes containing its acquisition parameters and the CAMAC response byte	IN b1,b2,r

3. THEORY OF OPERATION

3.1 General

The Model 8901A is a GPIB to CAMAC interface which is composed of two circuit boards. The first board plugs into the control (rightmost) slot of the CAMAC mainframe and interfaces to the CAMAC station number (N) lines and LAM lines. This board also contains the GPIB interface circuitry. The second board provides the interface to the CAMAC Dataway. It has registers to store the CAMAC commands sent by the GPIB controller and drive the function (F), address (A), and write data (W) lines of the Dataway during a CAMAC cycle. It also has the circuit to generate the CAMAC cycle timing and latch the read data (R) lines.

The 8901A circuitry can be broken down into logical subsections as shown in the attached block diagram. The operation of each of these subsections is discussed below. Schematics are also included.

3.2 GPIB Command Decoder

At the heart of the 8901A is the GPIB command decoder. When a command is put on the GPIB bus it must be interpreted by the 8901A and a decision must be made as to how (if at all) to respond to it. The 8901A will respond to any of the following GPIB commands: interface clear (IFC), serial poll enable (SPE), serial poll disable (SPD), my Talk address (MTA), my Listen address (MLA), Unlisten (UNL), and Untalk (UNT).

The 8901A has four basic states: Idle, Talk mode, Listen mode, Serial poll mode. These states are entered and exited as a result of one of the above GPIB commands. The following table lists each of the commands and describes its effect on the 8901A's state.

IFC - Resets all registers in the 8901A and places it in the Idle state regardless of its current state

SPE - Causes the 8901A to enter Serial Poll mode

SPD - If the 8901A is in Serial Poll mode, this command returns it to the Idle state. It also clears a pending service request (SRQ)

MTA - If in Serial Poll mode, the 8901A will output its SRQ status upon receiving its Talk address. If not in Serial Poll mode, receipt of MTA will cause a CAMAC cycle to be executed and Talk mode to be entered.

UNT - Takes the 8901A out of Talk mode if it is active MLA - Causes the 8901A to enter Listen mode so that it may accept CAMAC or setup commands.

UNL - Places the 8901A into the Idle state if currently in Listen mode.

3.3 Acceptor Handshake

The GPIB protocol provides a handshake for all data transfers. When a GPIB command is sent or the 8901A is in Listen mode, the 8901A must indicate that it is ready to receive a transfer by asserting the RFD line. The GPIB controller must then assert DAV when valid data is on the bus. The 8901A can then read in the data. It then asserts the DAC line to say the transfer is complete.

3.4 Listen Mode

Bits 6 and 7 of the first byte the 8901A receives from the GPIB Talker after entering Listen mode is used to determine whether the byte is a command for the 8901A itself, a "global" CAMAC command or a CAMAC command for a specific module. Bits 1-5 are then latched in the appropriate registers. If it's a CAMAC F command for a particular instrument, a sequencer is used to latch additional bytes in the following order: A, N, W1-8, W9-16, W10-24.

3.5 Global CAMAC Commands

There are three global CAMAC commands: C, Z, and I. For each of these commands there is a corresponding line on the CAMAC Dataway which is driven by the 8901A whenever a CAMAC cycle is executed. The command is asserted if its latched value is a 1. At the end of the CAMAC cycle the C and Z latch is reset to zero.

3.6 F, A, N CAMAC Commands

As described above, the values for F, A, N, and the Write data are latched when the information is sent from the GPIB controller. When a CAMAC cycle is executed, all of these lines are driven for the entire length of the cycle (while Busy is asserted). The latched values will not change until they are overwritten by a new command from the GPIB controller.

3.7 8901A Commands

The commands for the 8901A determine how many bytes are to be read back, whether a new CAMAC cycle should be executed when data is read out (block mode), and what conditions (if any) should cause SRQ to be asserted by the 8901A. The latches for this information are cleared if an IFC is sent. The block transfer enable flip flop also is cleared when a Q = 0 is read in.

3.8 Serial Poll Mode

Serial poll is used by the GPIB controller to determine which device asserted SRQ. Upon decoding the serial poll enable command, the SPAS flip flop is set true, putting the 8901A in serial poll mode. When the controller then addresses the 8901A to Talk, the serial poll status bytes are sent instead of data and CAMAC cycles are inhibited.

Bit 7 of the status bytes indicates the state of the SRQ line while bits 1-6 are used for data. The first byte contains X and Q, while the next 4 bytes contain the LAM status (six slots/byte) starting with slot 1. The SRQ is cleared when all of the status is read out or when the 8901A receives a serial poll disable command.

3.9 Talk Mode

When the 8901A is addressed to Talk (and serial poll mode is not active) two things occur. First, the 8901A enters the Talker active state. This causes the direction of the GPIB buffers to be reversed, since the 8901A must now drive the GPIB bus and it must disable the acceptor handshake circuit and enable the source handshake circuit. Secondly, the 8901A starts the execution of a CAMAC cycle. Upon completion of the cycle the appropriate number of data bytes are sent to the GPIB Listener followed by the X and Q response byte which is sent with the EOI signal asserted.

3.10 Source Handshake

Since the 8901A is in Talk mode, the GPIB handshaking protocol reverses. That is, the 8901A is now the one to indicate when data is valid. Three conditions must be met before it can assert DAV. First, it must be in Talk mode and ATN must be set false by the GPIB controller. Also it must wait for the GPIB controller (or Listener) to assert RFD. The last condition is that the CAMAC data must be latched into the 8901A during the CAMAC cycle. When all of these conditions have been met, the 8901A waits an additional 200 nsecs before asserting DAV to allow time for the data to become stable on the GPIB bus. When the listening device asserts DAC, DAV is cleared and a sequencer is clocked to output the next byte. This byte may be another data byte, or a status byte. If in block mode the status byte is suppressed, and a new CAMAC cycle is initiated instead.

3.11 CAMAC Cycle Timing

The CAMAC cycle starts when the 8901A is addressed to Talk or, if it is in block mode transfer, when the last data byte is read out. The 8901A asserts the Busy line and enables the F,A,N,W,C,Z and I drivers. Approximately 500 nsecs later, S1 is asserted for 250 nsecs. At the end of S1, all 24 bits of the CAMAC data lines, X, and Q are latched in the 8901A. S2 is asserted 125 nsecs later for 250 nsecs. The cycle is terminated 125 nsecs after S2 goes away, Busy is cleared and all drivers are disabled.

3.12 Read Data

The sequencer described above determines which data byte is to read out. The order of the first two bytes may be reversed by side-panel jumpers. The data is latched in the 8901A on every CAMAC cycle and generally read out immediately after the cycle completes. However, a special command (F(0), A(0), N(24)) is provided to allow readout of the latched data (the CAMAC cycle is inhibited) at a later time.

3.13 X and Q Response

The X and Q responses are latched in the 8901A during the CAMAC cycle and read out in the response byte. They are also used in the generation of SRQ's and termination of block mode transfers.

3.14 LAM Lines

The LAM lines are used by the SRQ generation circuit and can be read by the GPIB controller when it's conducting a serial poll.

3.15 SRQ Generation

A service request (SRQ) may be generated (depending on how the 8901A is programmed) on any of the following conditions: a LAM is set by one of the CAMAC instruments, or a X = 0 or Q =0 response is detected during the execution of a CAMAC cycle. When a service request is pending, CAMAC cycles are inhibited until a serial poll is performed and the SRQ cleared. However, if the SRQ was caused by a LAM, unless the LAM is cleared or the 8901A is disabled to generate SRQ's on LAM before the serial poll is taken, another SRQ will be issued immediately.

APPENDIX A

DESCRIPTION OF CAMAC

CAMAC modules may be plugged into a CAMAC mainframe (called Crate in the CAMAC standard) which has up to 25 Stations numbered 1 through 25. A station is a slot which accepts a CAMAC module. Some modules occupy several stations. The rightmost two stations are reserved for a Crate Interface or Controller whereas the remainder are Normal Stations used for instrumentation modules. The purpose of the crate controller is to issue CAMAC Commands to the modules and transfer information between a computer and the CAMAC modules. It is the interface between the CAMAC Dataway and a computer.

All CAMAC operations take place over the CAMAC Dataway. The Dataway is a parallel bus used to transfer all (of the) data, the function coding information, and all status information. In a typical Dataway operation, the crate controller issues a CAMAC Command which incudes specifying a station number (N), a subaddress (A), and function code (F). In response, the module will generate a valid command accepted (X response) and act on the command. If this command requires data transfer, the read (R) or write (W) lines will be used. Note that the terms Read and Write apply to the crate controller, not the module. For example, under a read command, the crate controller reads data contained within a module.

Whenever there is no Dataway operation in progress (indicated by the absence of the Busy signal) any module may generate a signal on its individual Look-at-Me line to indicate that it requires attention. Three common control signals are available without address by a command at all stations, in order to initialize all units, to clear data registers, and to inhibit features such as data-taking.

Definition of CAMAC Commands

The CAMAC command consists of signals on the Dataway lines which specify at least one module (by individual station number lines), a subsection of the module or modules (by the four subaddress bus lines), and the function to be performed (by the five function bus lines). The command signals are maintained for the full duration of the operation on the Dataway.

Station Number (N): Each normal station is addressed by a signal on an individual station number line (N) which comes from a separate pin at the control station.

Subaddress Codes (A8, A4, A2, A1) Different sections of a module are addressed by signals on four A bus lines. These signals are decoded in the module to select one of up to 16 subaddresses, numbered in decimal from A(0) to A(15).

Function Codes (F16, F8, F4, F2, F1): The function to be performed at the specified subaddress in the selected module or modules is defined by the signals on the five F bus lines. These signals are decoded in the module to select one of up to 32 functions, numbered in decimal from F(0) to F(31). To see what functions a particular LeCroy instrument reacts to, see its manual.

CAMAC Data

A common parallel highway is used for all data transfers. All information carried by the parallel highway is conveniently described as data, although it may be information concerned with status or control features in modules. Up to 24 bits may be transferred in parallel between the controller and the selected module. Independent lines (Read and Write) are provided for the two directions of transfer.

The Write Lines (W1-W24): The crate controller generates data signals on the 24 parallel W bus lines at the beginning of any Write operation.

The Read Lines (R1-R24): Data signals are set up on the 24 parallel R bus lines by the instrumentation module as soon as a Read command is recognized. The Model 8901A strobes data from the R bus lines into its own internal registers, whereafter the data is appropriately formatted for GPIB compatible transfers.

CAMAC Status Information

CAMAC status information is conveyed by signals on the Look-at-Me (LAM), Busy (B), Response (Q) and Command Accepted (X) lines. This status information is similar to the GPIB service request.

Look-at-Me (LAM): This, like the N line, is an individual connection from each station to a separate pin at the control station. When there is no Dataway operation in progress (no B present) any plug-in

unit may generate a signal on its L line to indicate that it requires attention, such as is the case when a transient recorder has finished a conversion sequence. A Look-at-Me request can be reset by Clear Look-at-Me, Initialize, or by the performance of the specific action which generated the request.

Q Response (Q): The Q busline is used during a Dataway operation to transmit a signal indicating the status of a selected feature of the module, such as whether or not data being read is valid.

Command Accepted (X): Wherever a module is addressed during a command operation it must generate an X=1 on the Command Accepted busline if it recognizes the command as one that it is equipped to perform.

Common Controls and Signals

The following common control signals operate on all modules within the crate, without requiring address by a command.

Initialize (Z): The initialize signal has absolute priority over all other signals or controls. It sets all units to a basic state by resetting all registers, and by resetting all LAM signals and disabling them where possible. The technical data sheet indicates what effect the initialize command has for a particular LeCroy instrument.

Inhibit (I): The presence of this signal can be used by a module to inhibit any activity (for example, data-taking).

Clear (C): The common clear signal resets all registers or bistables connected to it.

APPLICATION NOTE

LeCroy

PROGRAMMING LeCROY GPIB MODULAR DIGITIZERS WITH A HEWLETT PACKARD 9836 DESKTOP COMPUTER

LeCroy modular waveform recorders allow high speed digitizing with sampling rates from KS/s to 200 MS/s, and long memory in a high density, flexible configuration. The modules are placed in either a benchtop or rackmount instrument mainframe, LeCroy Models 8013A and 1434A, respectively. The mainframes provide power and data communications to the digitizers and receive commands from the control module, Model 8091A, which rests in the most right slots of the mainframe. The 8901A GPIB module interprets instrument commands from the computer to all modules in the mainframe. Each GPIB bus instrument has a unique address for receiving/writing information. On the 8901A, the device address is set by a dip switch on the front panel of the module. Up to 23 independent programmable modules with assorted digitizing speeds and memory combinations may be configured in one Model 1434A mainframe, providing a high density multichannel GPIB acquisition device. Alternatively, a LeCroy mainframe/digitizer with Model 8901A can be integrated with other GPIB devices as a complex test and measurement system.

Programming of LeCroy Modules:

Modular recording products from LeCroy are programmed using three byte sequences sent from the computer to the 8901A and are defined below:

N: Station Number - Defines the slot where the digitizing module is inserted. On the Model 8013A, N can range from 1 to 11; on the 1434A N ranges from 1 to 23.

F: Function Command - Gives primary action to be performed by module.

A: Sub-Address - Provides sub-commands to address different sections of module (e.g., channel number).

The following are working examples of programming the LeCroy Model TR8828C 200 MS/s or TR8818 100 MS/s modular recorders using the Model 8901A and the HP9836 desktop computer. HP BASIC Version 3.0 was used for writing the code. Additional and complete function commands for the digitizers and 8901A interface are contained in the respective manuals.

Highlights of 8901A and Digitizer Programming:

The 8901A was set to a device address of 1 and called from the HP code as device 701, as shown below:

```
OUTPUT 701 USING "#, B"; 17, 0, 8
```

The "#, B" sets the format of data as BINARY. In this example, the F=17 command A=O, N=slot 8 sets the data pointer back to the beginning of memory prior to reading out memory.

Sending a command to a digitizer is done in the CAMO subroutine, lines 10000 to 10091. Note that upon programming a module, a talk byte (line 10080) is sent to the 8901A to initiate a cycle in the instrument mainframe. Function code, sub-address, slot and bytes are predefined for setup, arming, triggering, and reading setting memory pointer to beginning. Upon entering the CAMO subroutine the bytes are sent over the GPIB. Figure 1 illustrates the sequence of operations used to program a recorder. Upon filling memory, a LAM (Look At Me) flag is initated to the 8901A for the digitizer slot. A service request (SRQ) is sent to the HP9836. A Serial Poll Service Subroutine (lines 10100 to 10190) is initiated to handle the SRQ, read 5 Status Bytes from the 8901A, and clear the LAM.

Data transfer is programmed in lines 10400 to 10419. Note that since the TR8818 and TR8828C send out 2 bytes in the mainframe, lines 10420 to 10449 are used to restore data and convert data to integers, that can be plotted on the computer screen.

In addition to programming modules using F-A-N commands in the CAMO section, decimal bytes are used to program the 8901A module for the form of data to send over the bus. For example, line 10413 programs the 8901A module for high speed block reads of data by transmitting byte 106. When in block read mode a single Function Command of 2 sent to the digitizer initiates a data read from the recorder until memory has been depleted.

The same output subroutine used for digitizers is used to program other LeCroy modules, such as a signal conditioner, clock generator module, or gate and delay generator. The set of function commands defined for each module are inserted to obtain the desired state of operation.

A detailed listing of the above program follows along with comments explaining each subroutine and statement.

SAMPLE PROGRAM LOOP

```
┌─→ F9          ARM
│
│   F27         CHECK LAM, INTERPRET STATUS BYTES
│
│   F25         COMPUTER GENERATED TRIGGER
│
│   F17         SET MEMORY TO ZERO
│
│   OUT 106     HIGH SPEED TRANSFER MODE ON 8901A
│
└── F2          READ DATA
```

FIGURE 1

```
!  TR8K_16ST!
!
!*****************************************************************************
!                THIS PROGRAM READS OUT A TR8828 USING AN 8K "TRANSFER"
!                IN HIGH SPEED BLOCK READ MODE 16 BIT TRANSFERS
! ************  EACH POINT IS READ INTO A STRING VARIABLE **********
! ************  THEN CONVERTED TO AN INTEGER ******************
!*****************************************************************************
!
ON KBD GOSUB Gsrid
Flag=1                                  !GRID ON OFF FLAG
ASSIGN @Gpib TO 701
!
PRINT CHR$(12)                          ! CLEAR SCREEN
GCLEAR
CLEAR 7                                 !CLEAR GPIB
CLEAR 701
!
PRINT "        Samplins Period"
PRINT "-------------------------------------------------------------------"
PRINT "        1 = 5ns                  5 = 80ns"
PRINT "        2 = 10ns                 6 = 160ns"
PRINT "        3 = 20ns                 7 = 320ns"
PRINT "        4 = 40ns                 8 = EXT CLK"
!
PRINT
PRINT
INTEGER Pretris                         !DECLARE INTEGER
INTEGER N,F,A,Dat1,Dat2,mask
A=0
!
INPUT "ENTER SLOT NUMBER",N                     !GET SLOT NUMBER
INPUT " ENTER SAMPLING PERIOD : ",Clk           !GET SAMPLE CLOCK
IF Clk<1 THEN 170
IF Clk>8 THEN 170
PRINT
INPUT " ENTER n/8 PRE-TIGGER SAMPLES : ",Pretris
IF Pretris<0 THEN 230
IF Pretris>8 THEN 230
INPUT "A(uto) or E(xternal) STOP TRIGGER ? :",Mode$
!
OUTPUT 701 USING "#,B";33               !SEND Z TO INITIALIZE CRATE
!
Clk=Clk-1
Dat1=Pretris*(Clk*16)
Dat2=0                          !SET UP CONTROL WORD (FIXED 16K MEMORY SIZE)
F=16
GOSUB Camo                              !WRITE OUT CONTROL WORD
!
Start!                          !
!
!
!
F=10
GOSUB Camo                              !CLEAR LAM
F=24
GOSUB Camo                              !DISABLE LAM
!
!
F=19
Dat1=128
GOSUB Camo                              !WRITE OUT ZERO INPUT OFFSET
!
F=26                            !ENABLE LAM
GOSUB Camo
```

```
287   !
288   F=9                                   !START DIGITIZER
290   GOSUB Camo
292   !
293   !
294   IF Mode$="A" THEN Iris                !IF "A" THEN ISSUE STOP TRIGGER
295   GOTO 301
296 Iris:                  !
297   F=25
298   GOSUB Camo                            !SEND COMPUTER STOP TRIGGER
299   !
301   OUTPUT 701 USING "#,B";65             !ENABLE SRQ
302   !
303   ON INTR 7 GOTO Getdata  !Serpol       !ENABLE INTERUPT
304   ENABLE INTR 7;2
305   GOTO 305                              !SIT AND WAIT FOR INTERUPT
306   !
307 Getdata:                                !
308   GOSUB Serpol                          !GO TO SERIAL POLL SUBROUTINE
309   GOSUB Trans8K                         !GO READ DATA WITH A "TRANFER"
310   GOTO Plot8K                           ! GO PLOT DATA
401 !++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
10000 !**************************************************************************
10010 !
10020 !              SUBROUTINES ( CAMO ), ( SERPOL )
10030 !
10031 !       CAMAC OUTPUT SUBROUTINE ---  SERIAL POLL SERVICE SUBROUTINE
10040 !**************************************************************************
10050 !
10060 Camo:! SUBROUTINE CAMO
10070 OUTPUT 701 USING "#,B";F,A,N,Dat1,Dat2
10080 SEND 7;TALK 1          !TELL 8901 TO TALK
10090 RETURN
10091 !*********************************************************************
10100 !
10101 !
10110 !
10120 Serpol: ! SERIAL POLL ROUTINE  RETURNS STATUS OF CRATE
10130 ! at this point SRQ WILL HAVE BEEN ASSERTED
10140 !
10141 DISABLE INTR 7                        !DISABLE INTERUPTS
10145 INTEGER Stat1,Stat2,Stat3,Stat4,Stat5
10150 OUTPUT 701 USING "#,B";64             !DISABLE ANY FURTHER SRQ'S
10160 SEND 7;UNL mLA TALK 1 CMD 24          !CONFIGURE BUS AND SEND SPE
10170 ENTER 7 USING "#,B";Stat1,Stat2,Stat3,Stat4,Stat5  ! GET STATUS
10180 SEND 7;Cmd 25 UNT                     !SEND SPD AND UNTALK
10190 RETURN
10191 !
10192 !
10194 !**************************************************************************
10204 !
10390 !++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
10400 Trans8K:        !THIS SUBROUTINE WILL AQUIRE 8K OF DATA USING A "TRANSFER"
STATEMENT IN HIGH SPEED BLOCK TRANFER MODE 16 BIT READS
10401 !++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
10402 !
10403 !
10405 INTEGER Datbuf(8192) BUFFER
10406 DIM Tempbuf$[8192] BUFFER !READ DATA 8 BITS AT A TIME INTO STRING VARIABLE
10407 !
10408 ASSIGN @Buff TO BUFFER Tempbuf$;FORMAT OFF          ! DEFINE AN 8K BUFFER
10409 !
10410 F=17
10411 GOSUB Camo                             !RESET READ POINTER
10412 !
10413 OUTPUT 701 USING "#,B";106              !SET UP FOR HIGH SPEED BLOCK READ
```

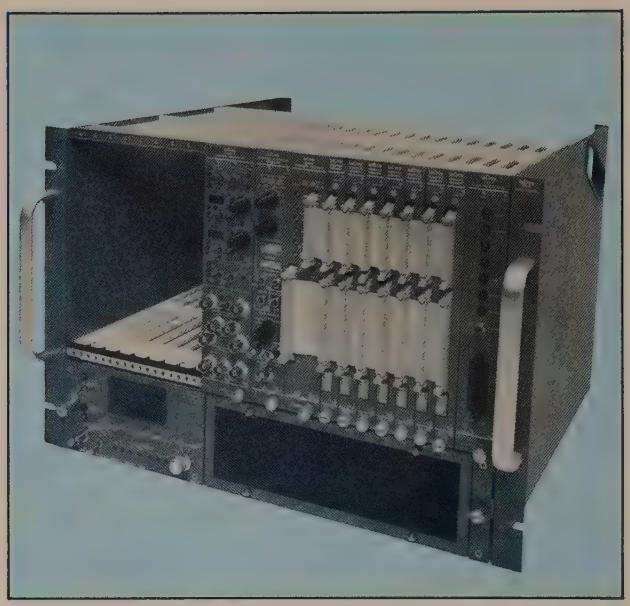
```
10414 OUTPUT 701 USING "#,B";2,0,N          !SEND OUT FIRST F2 COMMAND
10415 !
10416 TRANSFER @Gpib TO @Buff;END,WAIT                    ! TRANSFER 8K OF DATA
10417 !
10418 ASSIGN @Buff TO *
10419 !
10420 !!!!
```

```
30331 MOVE -1,Ylab
30332 LABEL USING "#,K";Ylab                    !LABEL Y AXIS
30333 NEXT Ylab
30334 Xlab=1024
30335 !
30336 FOR Xax=1350 TO 8518 STEP 1024
30337 MOVE Xax,-280
30338 LABEL USING "#,K";Xlab
30339 Xlab=Xlab+1024
30340 NEXT Xax
30342 !
30343 IF Datbuf(1)=0 THEN Bufpoint=16
30344 IF Datbuf(1)>0 THEN Bufpoint=17            !SET UP BUFFER POINTER
30345 !
30347 FOR P=Bufpoint TO 8176                    !DUMP FIRST AND LAST 16 POINTS
30350 PLOT P,Datbuf(P),1
30360 NEXT P
30361 SEND 7;UNT
30363 CLEAR 7
30368 GOTO Start
30370 END
```

APPLICATION NOTE

LeCroy

AN-33 INTRODUCTION TO CAMAC



Full power Crate with GPIB interface and waveform digitizer.

CAMAC is a modular data handling system used at almost every Nuclear Physics research laboratory and many industrial sites all over the world. It represents the joint specifications of the US NIM and the European ESONE Committees.

The primary application is data acquisition but CAMAC may also be used for remotely programmable trigger and logic applications (LeCroy ECLine family of programmable logic units). The CAMAC standard covers electrical and physical specifications for the modules, instrument housings or crates, and a crate backplane. Examples of crates include the LeCroy Model 1434A with 25 positions and the Model 8013A with 13 positions.

Individual crates are controlled by slave or intelligent controllers such as the LeCroy Model 4801. The controllers are tied together with a parallel Branch Highway that ends in a Branch Driver. The Branch Driver is interfaced directly to a data acquisition computer. Alternatively, tree or parallel data acquisition architectures may be created by connecting secondary CAMAC branches via an intelligent, programmable CAMAC Branch Driver Module, the Model 4805. This unit would reside in a crate on the primary CAMAC branch. See application note AN-35 for examples.

CAMAC crates may also be connected in a Local Area Fiber Optic Network via the LeCroy Model 5211 Fiber Optic Serial Link and a serial crate controller. Up to 62 crates separated by a maximum of 500 m can exchange data at transmission rates of 45 megabytes/sec.

LeCroy also offers crate controllers that interface directly with the GPIB or IEEE Std 488-1978 Bus. Therefore an entire CAMAC Crate may appear as a single instrument on this very popular laboratory instrument bus. The Model 8901A is a GBIP/CAMAC slave interface that operates as a "Talker/Listener" while the Model 4802 may be programmed to do computations and data compaction.

Timing and protocol specifications permit up to 1 megaword/sec transfers of 16 or 24-bit words for both the DATAWAY and CAMAC Branch. GPIB timing is usually limited by the host computer and typically runs at 500 kilobytes/sec.

Corporate Headquarters: 700 South Main Street, Spring Valley, NY 10977, USA. Tel: (914) 578-6013, TWX: 710-577-2832

European Headquarters: Route du Nant-d'Avril 101, 1217 Meyrin 1-Geneva, Switzerland. Tel: (022) 82 33 55, Telex: 28230

SECTION 1: INTRODUCTION

CAMAC is an international standard of modularized electronics as defined by the ESONE Committee of the JRC, Ispra. Its function is to provide a scheme to allow a wide range of modular instruments to be interfaced to a standardized multi-receptacle which, in turn, may be interfaced to a computer. In this way, additions to a data transfer and control system may be made by plugging in additional modules and making suitable software changes. Thus, CAMAC allows information to be transferred into and out of the instrument modules.

CAMAC modules may be plugged into a CAMAC Crate which has 25 *STATIONS*, numbered 1 through 25. Station 25, the rightmost station, is reserved for a CRATE CONTROLLER, whereas Stations 1 — 24 are *NORMAL STATIONS* used for CAMAC Modules (see figure below). Usually, Station 24 is also used by the controller in that most controllers are double width (#2 CAMAC). The purpose of the controller is to issue CAMAC *COMMANDS* to the modules and transfer information between a computer (or other digital device) and the CAMAC modules.

Data transfer, control functions, and module powering is affected via the *DATAWAY.* This is a series of bus and individual lines across the back of the crate. The DATAWAY lines include digital data transfer lines, strobe signal lines, and addressing lines and control lines. See Table 3 for a pin allocation chart.

In a typical DATAWAY operation, the crate controller issues a CAMAC *COMMAND* which includes specifying a station number (N), a subaddress (A), and function code (F) (see Table 1). In response, the subaddress of the module will generate valid command accepted (X response) and act on the command. If this command requires data transfer, the read (R) or write (W) lines will be used. Note that the terms Read and Write apply to the controller, not the module. For example, under a Read command, the controller reads data contained within a module.

SECTION 2: USE OF THE DATAWAY LINES

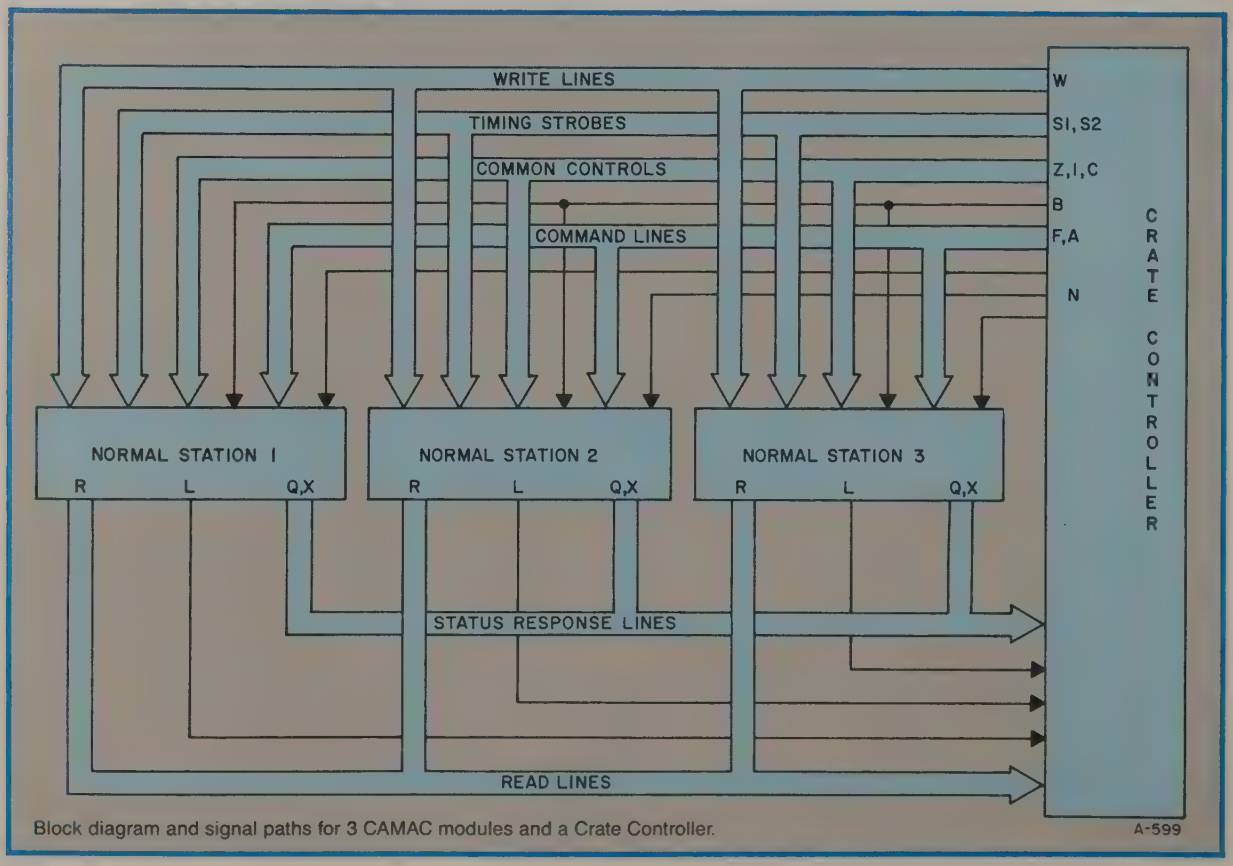
Communication with plug-in units takes place through the DATAWAY. This passive multi-wire highway is incorporated in the crate and links the 86-pin sockets to all stations. The bus lines link corresponding pins at all normal stations and, in some cases, the control station. Individual lines link one pin at a normal station to one pin at the control station. The patch pins have no specified DATAWAY wiring but can be connected to individual points to which patch leads may be attached.

During a DATAWAY operation the controller generates a command consisting of signals on individual Station Number lines to specify one or more modules, signals on the Subaddress bus lines to specify a sub-section of the module or modules, and signals on the Function bus lines to specify the operation to be performed. The command signals are accompanied by a signal on the Busy bus line, which is available at all stations to indicate that a DATAWAY operation is in progress.

When a module recognizes a Read command calling for a data transfer to the controller, it establishes data signals on the Read bus lines. When a controller recognizes a Write command calling for a data transfer to a module, it establishes data signals on the Write bus lines. In addition, regardless of whether there is transfer on the R or W lines, the module may transmit one bit of status information on the Response bus line.

Two timing signals, Strobes S1 and S2, are then generated in sequence on separate bus lines. The strobes are used to transfer data from the DATAWAY into modules (on Write commands) and into the controller (on Read commands). They may also initiate other actions within the controller and modules.

Whenever there is no DATAWAY operation in progress (indicated by the absence of the Busy signal) any module may generate a signal on its individual Look-at-Me line to indicate that it requires attention. Three common control signals are available



Block diagram and signal paths for 3 CAMAC modules and a Crate Controller.

A-599

at all stations, without requiring addressing by a command, in order to initialize all units (typically after switch-on), to Clear data registers, and to inhibit features such as data-taking.

2.1 DEFINITION OF COMMANDS

A command consists of signals on the DATAWAY lines which specify at least one module (by individual station number lines), a subsection of the module or modules (by the four subaddress bus lines), and the function to be performed (by the five function bus lines). The command signals are maintained for the full duration of the operation on the DATAWAY. They are accompanied by a signal on the Busy bus line which indicates to all units that a DATAWAY operation is in progress.

Station Number (N)

Each normal station is addressed by a signal on an individual station number line (N) which comes from a separate pin at the control station. The stations are numbered in decimal code from the lefthand end as viewed from the front, beginning with Station 1.

Subaddress (A8, A4, A2, A1)

Different sections of a module are addressed by signals on the four A bus lines. These signals are decoded in the module to select one of up to sixteen subaddresses, numbered in decimal from 0 to 15.

Function (F16, F4, F2, F1)

The function to be performed at the specified subaddress in the selected module or modules is defined by the signals on the five F bus lines. These signals are decoded in the module to select one of up to 32 functions, numbered in decimal from 0 to 31. The definitions of the 32 function codes are summarized in the DATAWAY Command Operations section.

Strobe Signals (S1 and S2)

Two strobe signals S1 and S2 are generated in sequence on separate bus lines. These signals are used to transfer information between plug-in units via the DATAWAY or to initiate operations within units. In either case the specific action is determined by the command present on the DATAWAY. Both strobes are generated during each DATAWAY command operation, and all plug-in units which accept information from the DATAWAY do so in response to these strobes. The first strobe S1 is used for actions which do not change the state of signals on the DATAWAY lines. All units which accept data from the DATAWAY in a Read operation, or in a Write operation do so in response to S1. The second strobe S2 is used to initiate any actions which may change the state of DATAWAY signals, for example, clearing a register whose output is connected to the DATAWAY.

2.2 DATA

A common parallel highway is used for all transfers. All information carried by the parallel highway is conveniently described as data, although it may be information concerned with status or control features in modules. Up to 24 bits may be transferred in parallel between the controller and the selected module. Independent lines (Read and Write) are provided for the two directions of transfer.

The Write Lines (W1-W24)

The controller or other common data source generates data signals on the W bus lines at the beginning of any "Write" operation. The W signals reach a steady state before S1, and are maintained until the end of the operation, unless modified by S2.

The Read Lines (R1-R24)

Data signals are set up on the R bus lines by the module as soon as a "Read" command is recognized. The R signals reach a steady state before S1, and are maintained for the full duration of the DATAWAY operation, unless the state of the data source is changed by S2. The controller or other common data receiver strobes the data from the R bus lines at the time of the Strobe S1.

2.3 STATUS INFORMATION

Status information is conveyed by signals on the Look-at-Me (L), Busy (B), and Response (Q) lines.

Look-at-Me (L)

This, like the N line, is an individual connection from each station to a separate pin at the control station. When there is no DATAWAY operation in progress (no B present) any plug-in unit may generate a signal on its L line to indicate that it requires attention. When B is present each L signal is gated off the DATAWAY line by the unit which generates it.

A Look-at-Me request can be reset by Clear Look-at-Me, initialize, or by the performance of the specific action which generated the request.

DATAWAY Busy (B)

The Busy signal is used to interlock various aspects of a system which can compete for the use of the DATAWAY. Specifically, it is generated during DATAWAY command or common control operations. Whenever N is present, B is present, and for the duration of B, all L signals are gated off the DATAWAY lines.

Response (Q)

The Q bus line is used during a DATAWAY operation to transmit a signal indicating the status of a selected feature of the module.

On all Read and Write commands the signal on the Q bus line remains static from the time the command is received until S2. For all other commands the signal on the Q bus line may change at any time.

2.4 COMMON CONTROLS

Common control signals operate on all modules connected to them without the need to be addressed separately by a command. In order to provide protection against spurious signals, the initialize (Z) and Clear (C) signals must be accompanied by Strobe S2.

Initialize (Z)

The initialize signal has absolute priority over all other signals or controls. It sets all units to a basic state by resetting all registers, whether data or control, to a defined state, and by resetting all L signals and disabling them where possible. Units which generate Z must also cause S2 and B to be generated. Modules which accept Z gate it with S2 as a protection against spurious signals on the Z line.

Inhibit (I)

The presence of this signal inhibits any activity (for example, data taking). It must either not change when B is present or have rise and fall times not less than 200 nsec.

Clear (C)

This command signal clears all registers or bistables connected to it. Units which generate C must also cause S2 and B to be generated. Modules which accept C gate it with S2 as a protection against spurious signals on the C line.

2.5 PRIVATE WIRING

Patch Leads (P1-P7)

Five pins (P1 to P5) on the 86-way socket at normal stations

are not prewired to DATAWAY lines but are freely available for local connections. At the control station, seven pins (P1-P7) are available. Signals on the patch pins must either remain static when B is present or have rise and fall times not less than 20 nsec.

2.6 DATAWAY COMMAND OPERATIONS

A Command is composed of signals on the Station Number line or lines, the Subaddress lines and the Function lines. It is accompanied by a signal on the Busy Line. In response to a command, data may be transferred on the Read or Write lines and one bit of status information on the Q line. The two Strobes S1 and S2 must be generated in each DATAWAY command operation to control its timing.

The order in which the commands are described below corresponds to the function codes set out in Table 1. In this table the term "register" is used for an addressable data source or receiver, without implying that it has a data storage property. The function codes allow the registers in a module to be divided into two distinct sets, known as Group 1 and Group 2. Thus it is possible to operate on more than the basic set of 16 registers selected by the four subaddress lines.

A common feature of all commands is that if the module has a Look-at-Me source which requests a specific command, then the performance of that command should reset the Look-at-Me source.

Read Commands (Function Codes 0-7)

Read commands are identified by the combination F16 = 0, F8 = 0 in the function code. They specify that information is to be transferred from a module to a controller via the R bus lines. Data signals are set up on the R bus lines by the module as soon as the "Read" command is recognized, and the appropriate status signal connected to the Q bus line. The R and Q signals reach a steady state before S1, and are maintained for the full duration of the DATAWAY command operation unless the state of the signal source is changed at S2. The controller or other common data receiver strobes the data from the R and Q bus lines at the time of the Strobe S1.

In order to facilitate reading by sequential addressing, all registers containing data (as opposed to control information) must have consecutive subaddresses starting at subaddress 0. At each of these subaddresses the module generates Q = 1 in response to the appropriate Read command. At the next subaddress in sequence (where there is not a data register) the response is Q = 0. At all remaining addresses the Q signal may be used to test any feature, subject to the general requirement that the Q signal must be static from the beginning of command until at least S2.

CODE 0, READ GROUP 1 REGISTER

This command selects, by subaddress, one register from the first group in the module and transfers the contents of this register to the controller. The contents of the register remain unchanged.

CODE 1, READ GROUP 2 REGISTER

Same as Code 0, except command selects register from the second group.

CODE 2, READ AND CLEAR GROUP 1 REGISTER

Same as Code 0, except the module register is cleared at time S2.

CODE 3, READ COMPLEMENT OF GROUP 1 REGISTER

Same as Code 0, except command transfers the complement of the contents of this register to the controller.

CODE 4-7

Unassigned at this time.

2.7 CONTROL COMMANDS (FUNCTION CODES 8-15)

Control commands are identified generally by F8 = 1 in the function code. They are divided into two groups by the state of F16, in this case F16 = 0. They specify that information is not transferred on either the R or W bus lines. However, information may be conveyed on the Q bus line in any of these commands. The signal on the Q bus line may change at any time but is strobed into the controller at time S1 and may (except in Code 8) be reset by Strobe 2.

CODE 8, TEST LOOK-AT-ME

This command selects a Look-at-Me source in the module and presents the state of this source on the Q bus line.

CODE 9, CLEAR GROUP 1 REGISTER

This command selects, by subaddress, a register from the first group in the module and clears the contents of this register.

CODE 10, CLEAR LOOK-AT-ME

Same as Code 8, except the Look-at-Me source is cleared at time S2.

CODE 11, CLEAR GROUP 2 REGISTER

Same as Code 9, except command selects register from the second group.

CODE 12-15

Unassigned at this time.

2.8 WRITE COMMANDS (FUNCTION CODES 16-23)

Write commands are identified by the combination F16 = 1, F8 = 0 in the function code. They specify that information is to be transferred from a controller to a module via the W bus line. The controller or other common data source generates data signals on the W bus lines at the beginning of the "Write" operation. The module connects the appropriate status signal to the Q bus line as soon as the command is recognized. The W and Q signals reach a steady state before S1 and are maintained for the full duration of the DATAWAY command operation unless the status of the signal source is changed at Strobe 2. In order to facilitate writing into registers by sequential addressing, all registers which are to contain data (as opposed to control information) have consecutive subaddress starting at subaddress 0. At each of these subaddresses, the module generates Q = 1 in response to the appropriate Write function. At the next subaddress in sequence (where there is not a data register), the response is Q = 0. At all remaining subaddresses the Q signal may be used to test any feature subject to the general requirement that the Q signal must be static from the beginning of the command until at least S2.

CODE 16, OVERWRITE GROUP 1 REGISTER

This command selects, by subaddress, one register in the first group in the module and sets the contents of this register to correspond with the data generated on the W bus lines by the controller.

CODE 17, OVERWRITE GROUP 2 REGISTER

Same as Code 16, except command selects a register in the second group.

CODE 18, SELECTIVE OVERWRITE GROUP 1 REGISTER

Same as Code 16, except a separate "mask" register defines which bits in the selected register are set.

CODE 19, SELECTIVE OVERWRITE GROUP 2 REGISTER

Same as Code 18, except command selects a register in the second group.

CODE 20 – 23

Unassigned at this time.

2.9 CONTROL COMMANDS (FUNCTION CODES 24-31)

Control commands are identified generally by F8 = 1 in the

function code. They are divided into two groups by the state of F16, in this case F16 = 1. They specify that information is not transferred on either the R or W bus lines. However, information may be conveyed by the Q bus line in any of these commands. The signal on the Q bus line is permitted to change at any time but is strobed into the controller at time S1 and may (except in Code 27) be reset by Strobe S2. Precautions must be taken to ensure that information is not lost due to Q signals appearing between S1 and S2.

CODE 24, DISABLE

This command selects, by subaddress, and disables a feature of the module; e.g., a Look-at-Me source or a data input.

CODE 25, INCREMENT PRESELECTED REGISTERS

This command adds one simultaneously to the contents of each register in one of 16 groups, defined by the subaddress.

CODE 26, ENABLE

This command enables the feature of the module selected by the subaddress, e.g., a Look-at-Me source or a data input.

CODE 27, TEST STATUS

This command selects, by subaddress, any feature of a module other than a source of a Look-at-Me request, and tests it by producing a response on the Q bus line.

CODE 28 – 31

Unassigned at this time.

CAMAC Reference Data

CAMAC FUNCTION CODES

CODE F( )	FUNCTION	FUNCTION SIGNALS F16	F8	F4	F2	F1	CODE F( )
0	Read Group 1 Register	0	0	0	0	0	0
1	Read Group 2 Register	0	0	0	0	1	1
2	Read and Clear Group 1 Register	0	0	0	1	0	2
3	Read Complement of Group 1 Register	0	0	0	1	1	3
4	Non-standard	0	0	1	0	0	4
5	Reserved	0	0	1	0	1	5
6	Non-standard	0	0	1	1	0	6
7	Reserved	0	0	1	1	1	7
8	Test Look-at-Me	0	1	0	0	0	8
9	Clear Group 1 Register	0	1	0	0	1	9
10	Clear Look-at-Me	0	1	0	1	0	10
11	Clear Group 2 Register	0	1	0	1	1	11
12	Non-standard	0	1	1	0	0	12
13	Reserved	0	1	1	0	1	13
14	Non-standard	0	1	1	1	0	14
15	Reserved	0	1	1	1	1	15
16	Overwrite Group 1 Register	1	0	0	0	0	16
17	Overwrite Group 2 Register	1	0	0	0	1	17
18	Selective Set Group 1 Register	1	0	0	1	0	18
19	Selective Set Group 1 Register	1	0	0	1	1	19
20	Non-standard	1	0	1	0	0	20
21	Selective Clear Group 1 Register	1	0	1	0	1	21
22	Non-standard	1	0	1	1	0	22
23	Selective Clear Group 2 Register	1	0	1	1	1	23
24	Disable	1	1	0	0	0	24
25	Execute	1	1	0	0	1	25
26	Enable	1	1	0	1	0	26
27	Test Status	1	1	0	1	1	27
28	Non-standard	1	1	1	0	0	28
29	Reserved	1	1	1	0	1	29
30	Non-standard	1	1	1	1	0	30
31	Reserved	1	1	1	1	1	31

TABLE 1

2.10 DIGITAL SIGNAL STANDARDS ON THE DATAWAY

The potentials for the binary digital signals on the DATAWAY lines have been defined to correspond with those for compatible current sinking logic devices (e.g., the TTL and DTL series). The signal convention has, however, been inverted to be negative logic. The high state (more positive potential) corresponds to logic '0' and the low state (near ground potential) corresponds to logic '1'. Intrinsic OR outputs are thus available from the manufacturers' standard product range, and disconnected inputs go to the '0' state.

It is an essential feature of the DATAWAY that many units may have their signal outputs connected to the Read and Response lines. Outputs onto these lines therefore require intrinsic OR gates. The same principle is extended to other lines (Command, Write, etc.) in order to allow more than one control-line unit in a crate. The Inhibit line may be an exception, since its signals are shaped with a slow rise and fall if they change during DATAWAY operations.

VOLTAGE STANDARDS FOR DATAWAY SIGNALS

All DATAWAY Signals must conform to the voltage levels as follows:

Pull-up current sources for all DATAWAY bus lines are located in the crate controller (occupying the control station and at least one other station) so as to insure that there is one and only one current source per line. The minimum pull-up current when the DATAWAY line is at + 3.5 V is defined as 2.5 mA. If the controller generates DATAWAY signals at time intervals near the permitted minima, the pull-up current sources should preferably provide not less than 6 mA when the lines are at this potential. The pull-up for the N signals is located in the unit generating the signals, and for the L signals in the unit receiving the signals, so that the individual lines may be joined or grouped within these units if desired.

The N and L lines are effectively individual lines joining two units (a module and a controller). The Q and R lines generally will have many units generating the signals (say 20) with a few units (maximum four) receiving the signals. The remaining lines (W, A, F, S, B, Z, I, C) will have relatively few units generating each signal (often only one) with the possibility of many units receiving the signals.

TIMING OF DATAWAY SIGNALS

The sequence of events during a single DATAWAY operation is shown in the Timing Diagram on the following page. The shaded areas indicate the permitted variation of each signal between an ideal square signal and a signal whose transition across the appropriate signal threshold (0.8 V or 2.0 V) satisfies the conditions shown. The signal waveforms for the command and data lines apply to those lines, if any, which take up the '1' state. Other command and data lines may, of course, be in the '0' state during the operation.

The signals on the Busy line and the various signals constituting the command need not occur in exact synchronism, provided their envelope lies within the shaded areas of the diagram. Similar variation is permitted between the signals constituting the data. The broken line indicates the earliest time at which the data signals may change in response to S2.

Key points on these waveforms are indicated by t_0 - t_9, with the following significance:

Points t_0, t_3, t_6 represent the initiation of the negative-going of the Command, Strobe 1, and Strobe 2 signals, respectively. They are the times at which the signals would be received from an ideal DATAWAY with no capacitative loading.

Points t_9, t_5, t_8 represent similarly the initiation of the positive-going edges of the same signals.

Points t_2, t_{11} are the latest time at which the data source is permitted to initiate the negative-going and positive-going edges of the data signals.

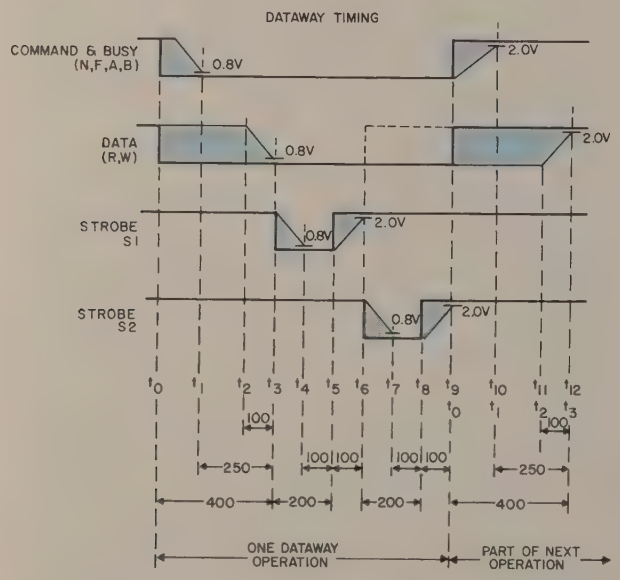
Points t_1, t_3, t_4, t_7 represent the latest times at which the received signals are permitted to reach a maintained '1' state, and therefore refer to the last negative-going transition across the +0.8 V threshold.

Points t_6, t_9, t_{10}, t_{12} represent the latest times at which the received signals are permitted to reach a maintained '0' state, and therefore refer to the last positive-going transition across the +2.0 V threshold.

Controllers must initiate the negative- and positive-going edges of the command and strobe signals at intervals not less than those defined by t_3, t_5, t_6, t_8, and t_9. Modules respond to the command within the most adverse value of (t_1 - t_2); i.e., 100 nsec. The electrical characteristics of the DATAWAY and connections from it into units must allow signals to rise and fall within the minimum times for (t_0 - t_1), (t_2 - t_3) etc.

The next DATAWAY operation must not start before t_9.

The extreme case is shown in the Timing Diagram below with the next operation starting at t_9; t_9 - t_{12} of one operation coincides with t_0 - t_3 of the next. The command and data signals of one operation may thus be removed while those of the next operation are being established. The Busy signal may be maintained continuously during a sequence of consecutive DATAWAY operations. Under suitable conditions any command or data signals of one operation may thus be removed while those of the next operation are being established. The Busy signal may be maintained continuously during a sequence of consecutive DATAWAY operations. Under suitable conditions any command or data signals which have the same state during successive operations may also be maintained. In the extreme case of successive operations with the same command and data, there could be a complete absence of signal transitions between t_0 and t_3.



Times given are maximum values in nsec timing of a Dataway operation.

SECTION 3: POWER SUPPLIES

The voltage tolerances and current loadings are specified in Table 2. The specified tolerances in voltage refer to the voltage measured at the contacts of the DATAWAY sockets and must be maintained under the worst combination of factors such as AC mains voltage and frequency, the maximum current loadings, temperature and the position in the crate of the socket under observation.

Note that the maximum currents stated in Table 2 below are subject to the overall restrictions as follows:

1. The current carried by any contact of the DATAWAY socket must not exceed 3 A.
2. The total power dissipated in a crate, without forced ventilation, must not exceed 200 W.
3. The power dissipation per single-width station should not, therefore, normally exceed 8 W. Under special circumstances, however, this rating may be increased to a maximum of 25 W, provided suitable precautions are taken to comply with total power dissipation and current loadings.

MAXIMUM CURRENT LOADS

SUPPLY VOLTAGE	VOLTAGE TOLERANCE	IN THE PLUG-IN (PER UNIT WIDTH) *See Notes 1 and 3 above.	IN THE CRATE *See Note 2 above
MANDATORY			
+24 V DC	±0.5%	1 A	6 A
+6 V DC	±2.5%	2 A	25 A
−6 V DC	±2.5%	2 A	25 A
−24 V DC	±0.5%	1 A	6 A
Additional (as required)			
+12 V DC	±0.5%		
+12 V DC			

Table 2

Bench Top 13 position Mini CAMAC Crate.

PIN ALLOCATION AT CONTROL STATION

(STATION 25)

Individual patch contact		P1	B	Busy	Bus line
Individual patch contact		P2	F16	Function	Bus line
Individual patch contact		P3	F8	Function	Bus line
Individual patch contact		P4	F4	Function	Bus line
Individual patch contact		P5	F2	Function	Bus line
Bus line	Command Accepted	X	F1	Function	Bus line
Bus line	Inhibit	I	A8	Subaddress	Bus line
Bus line	Clear	C	A4	Subaddress	Bus line
Individual patch contact		P6	A2	Subaddress	Bus line
Individual patch contact		P7	A1	Subaddress	Bus line
Bus line	Strobe 1	S1	Z	Initialize	Bus line
Bus line	Strobe 2	S2	Q	Response	Bus line
		L24	N24		
		L23	N23		
		L22	N22		
		L21	N21		
		L20	N20		
		L19	N19		
		L18	N18		
		L17	N17		
		L16	N16		
		L15	N15		
		L14	N14		
		L13	N13		
24 Individual Look-at-Me Lines		L12	N12	24 Individual Station	
L1 from Station 1, etc.		L11	N11	Number lines	
		L10	N10	N1 to Station 1, etc.	
		L9	N9		
		L8	N8		
		L7	N7		
		L6	N6		
		L5	N5		
		L4	N4		
		L3	N3		
		L2	N2		
		L1	N1		
	−12 V DC	−12	−24	−24 V DC	
			−6	−6 V DC	
Power	Auxiliary −6 V supply	Y1	E	Clean Earth	Power
Bus lines	−12 V DC	+12	+24	+24 V DC	Bus lines
	Auxiliary +6 V supply	Y2	+6	+6 V DC	
	0 V (Power Return)	0	0	0 V (Power Return)	

TABLE 3a

PIN ALLOCATION AT NORMAL STATION

(STATIONS 1-24)

Bus line	Free Bus line	P1	B	Busy	Bus line
Bus line	Free Bus line	P2	F16	Function	Bus line
Individual patch contact		P3	F8	Function	Bus line
Individual patch contact		P4	F4	Function	Bus line
Individual patch contact		P5	F2	Function	Bus line
Bus line	Command Accepted	X	F1	Function	Bus line
Bus line	Inhibit	I	A8	Subaddress	Bus line
Bus line	Clear	C	A4	Subaddress	Bus line
Individual line	Station Number	N	A2	Subaddress	Bus line
Individual line	Look-At-Me	L	A1	Subaddress	Bus line
Bus line	Strobe 1	S1	Z	Initialize	Bus line
Bus line	Strobe 2	S2	Q	Response	Bus line
		W24	W23		
		W22	W21		
		W20	W19		
		W18	W17		
24 Write Bus Lines		W16	W15		
W1=LSB		W14	W13		
W24=MSB		W12	W11		
		W10	W9		
		W8	W7		
		W6	W5		
		W4	W3		
		W2	W1		
		R24	R23		
		R22	R21		
		R20	R19		
		R18	R17		
24 Read Bus Lines		R16	R15		
R1=LSB		R14	R13		
R24=MSB		R12	R11		
		R10	R9		
		R8	R7		
		R6	R5		
		R4	R3		
		R2	R1		
	−12 V DC	−12	−24	−24 V DC	
			−6	−6 V DC	
Power	Auxiliary −6 V supply	Y1	E	Clean Earth	Power
Bus lines	−12 V DC	+12	+24	+24 V DC	Bus lines
	Auxiliary +6 V supply	Y2	+6	+6 V DC	
	0 V (Power Return)	0	0	0 V (Power Return)	

TABLE 3b

STANDARD DATAWAY USAGE

TITLE	DESIGNATION	CONTACTS	USE AT A MODULE
Command			
Station Number	N	1	Selects the module (Individual line from control station).
Sub-Address	A1, 2, 4, 8	4	Selects a section of the module.
Function	F1, 2, 4, 8, 16	5	Defines the function to be performed in the module.
Timing			
Strobe 1	S1	1	Controls first phase of operation. (Dataway signals may change).
Strobe 2	S2	1	Controls second phase (Dataway signals may change).
Data			
Write	W1-W24	24	Bring information to the module.
Read	R1-R24	24	Take information from the module.
Status			
Look-at-Me	L	1	Indicates request for service (Individual line to control station).
Busy	B	1	Indicates that a Dataway operation is in progress.
Response	Q	1	Indicates status of feature selected by command.
Command Accepted	X	1	Indicates that module is able to perform action required by the command.
Common Controls			Operate on all stations connected to them, no command required.
Initialize	Z	1	Sets module to a defined state. (accompanied by S2 and B).
Inhibit	I	1	Disables features for duration of signal.
Clear	C	1	Clears registers. (accompanied by S2 and B).
Non-Standard Connections			
Free bus-lines	P1, P2	2	For specified uses.
Patch contacts	P3-P5	3	For unspecified interconnections. No Dataway lines.
Mandatory Power Lines			
+24 V DC	+24	1	
+6 V DC	+6	1	
−6 V DC	−6	1	
−24 V DC	−24	1	
0 V	0	2	Power return
Additional Power Lines			Lines are reserved for the following power supplies
+12 V DC	+12	1	Low current for indicators, etc.
−12 V DC	−12	1	
Clean Earth	E	1	Reference for circuits requiring clean earth.
Reserved Y1, Y2	2		Reserved for future allocation.

TABLE 4

LeCroy

Innovators in Instrumentation

Corporate Headquarters:
700 South Main Street,
Spring Valley, NY 10977, USA
Tel: (914) 425-2000, TWX: 710-577-2832
European Headquarters:
Route du Nant d'Avril 101,
1217 Meyrin 1-Geneva, Switzerland
Tel: (022) 82 33 55, Telex: 28230
Sales and service offices throughout the world.

ADDENDUM 8901A 4/13/88

The following passage (indicated at left) should be updated to read as shown on the right.

Page 18

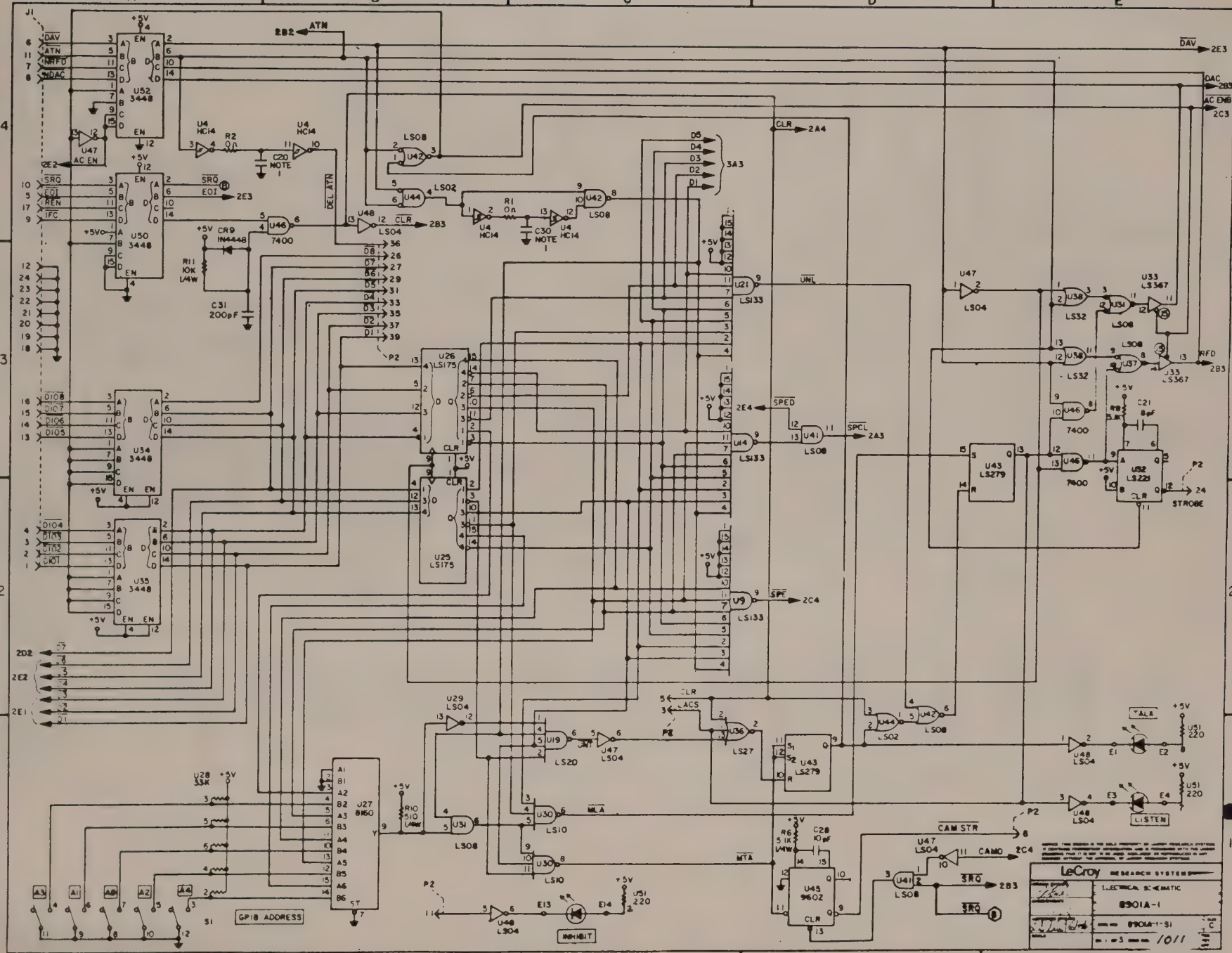
10427 FOR Fix=1 to 6192:

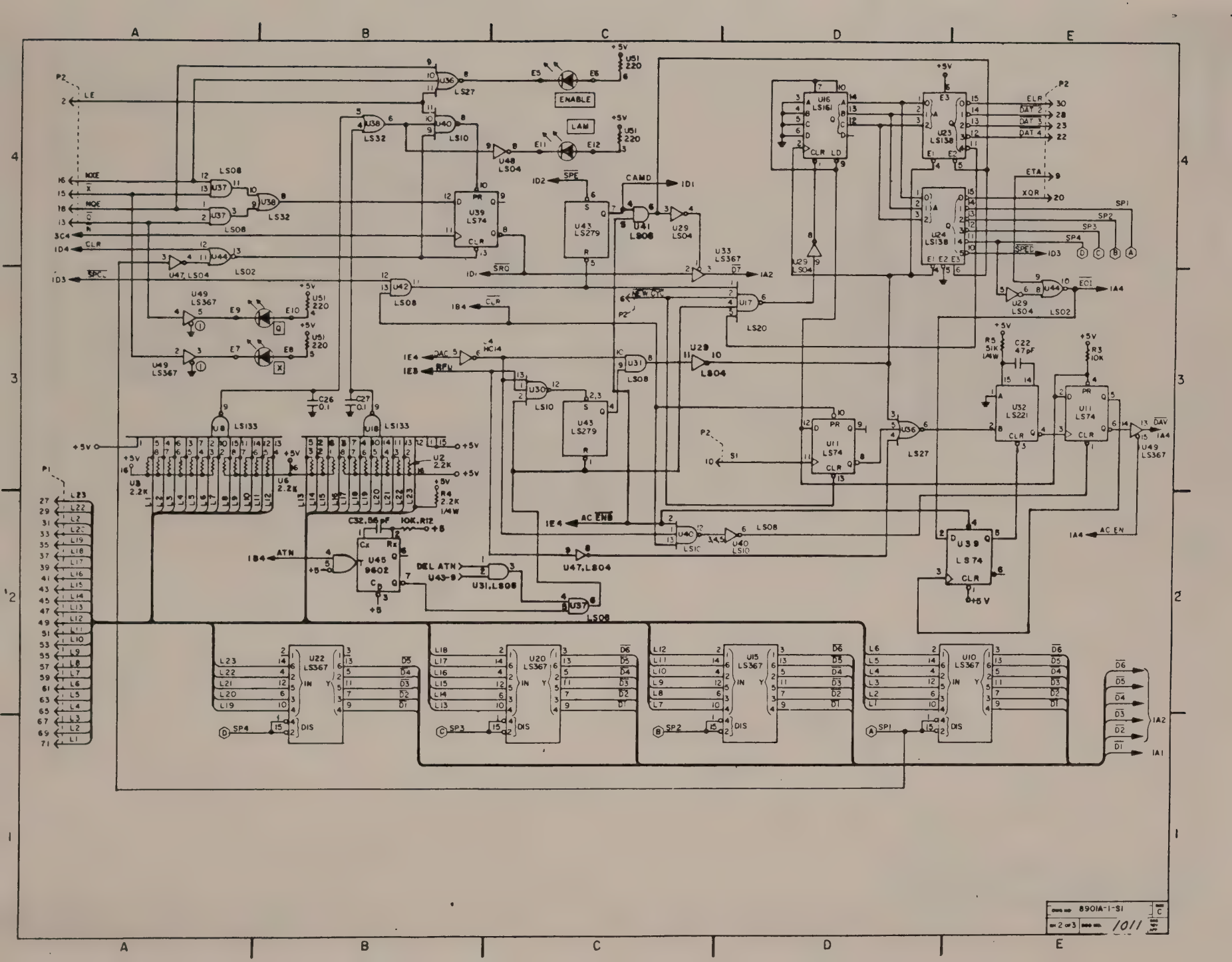
Replace line with **FOR Fix=1 to 8192**

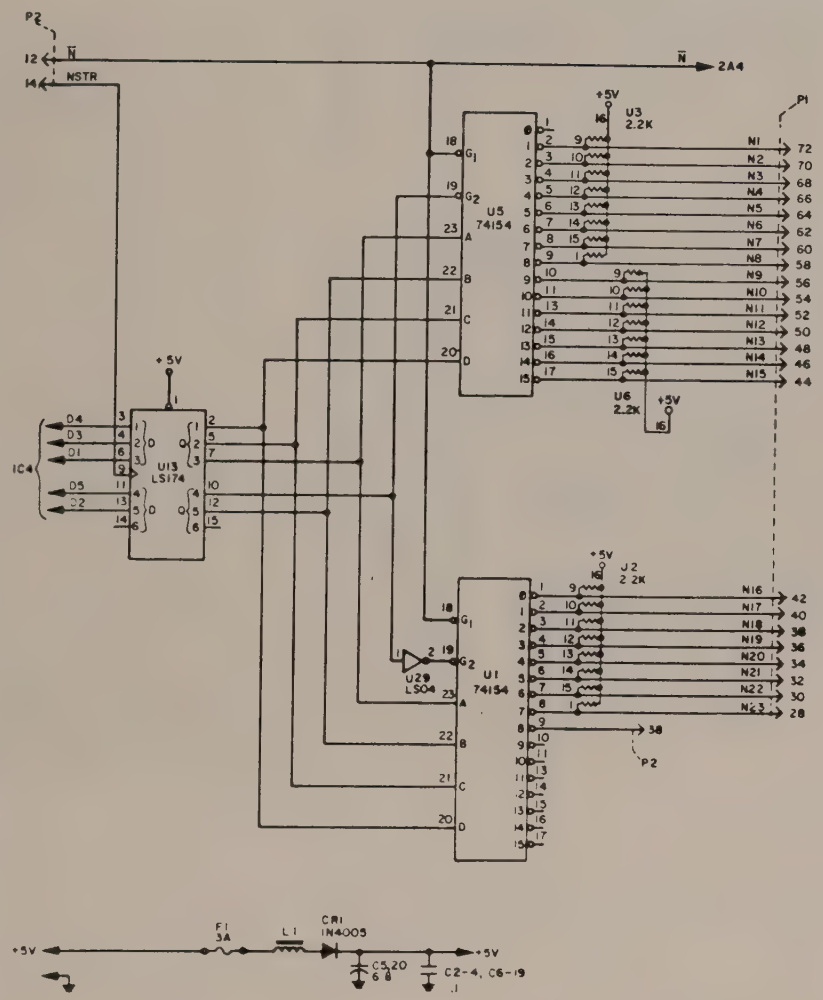
PART NUMBER	DESCRIPTION	QUANTITY PER
102444470	CAP CERA DISC 100V 47 PF	1
102444560	CAP CERA DISC 100V 56 PF	1
102745201	CAP CERA DISC 500V 200 PF	1
102944100	CAP CERA DISC 1KV 10 PF	1
103437104	CAP CERA MONO 100V .1 UF	19
116305180	CAP DIP MICA DM 5 18 PF	1
142824685	CAP TANT DIP CASE 6.8 UF	2
161030000	RES COMP ZERO OHMS	2
161225103	RES CARBON FILM 10 K	1
161225512	RES CARBON FILM 5.1 K	1
161335103	RES CARBON FILM 10 K	2
161335222	RES CARBON FILM 2.2 K	1
161335511	RES CARBON FILM 510 OHMS	1
161335512	RES CARBON FILM 5.1 K	1
161335513	RES CARBON FILM 51 K	1
190132222	RES NETWORK 2.2 K	3
190642333	RESISTOR NETWORK 33 K	1
190842221	RESISTOR NETWORK 220 OHMS	1
200031001	IC 2-INPUT NAND SN7400N	1
200031046	IC HEX INVERTER SN74LS04N	3
200031047	IC 3-INPUT NAND SN74LS10N	2
200031048	IC 4-INPUT NAND SN74LS20N	2
200031049	IC D-TYP FLOP SN74LS74N	2
200031051	IC 2-INPUT NOR SN74LS02N	1
200031057	IC 3-INPUT NOR SN74LS27N	1
200031073	IC 2-IN POS OR SN74LS32N	1
200031086	IC 2-INPUT AND SN74LS08N	4
200041026	IC 4-BIT CTR SN74LS161N	1
200041033	IC D-TYP FLOP SN74LS174N	1
200041039	IC MONO/MULTIVIB N74LS221	1
200041049	IC D-TYP FLOP SN74LS175N	2
200041057	IC LATCH SN74LS279N	1
200041059	IC BUS DRIVER SN74LS367N	6
200041062	IC DEC/DEMULTP SN74LS138N	2
200041064	IC MAGNITUDE COMP DM8160N	1
200041448	IC BIDIRECTNL BUS MC3448P	4
200042002	IC MULTIVIBRATOR 9602PC	1
200042007	IC 13-IN NAND 74LS133PC	5
200081001	IC DECODER/DEMUL SN74154N	2
200331014	IC HEX INVERTER MM74HC14	1
230110005	DIODE SWITCHING 1N4448	1
235010005	DIODE RECTIFIER 1N4005	1
256250200	LED CLR RED SUPER-BRIGHT	7
300050001	CHOKE FERRITE SINGLE LEAD	1
400230114	SOCKET IC VERTICAL DIP-14	1
403170040	HDR DBL ROW RT ANGL 40	1
405764007	SOCKET SINGLE WIRE CLOSED	2
411610001	SWITCH ROCKER PC MTG (6)	1
433220002	FUSE PICO II 125V 3 AMP	1
454622024	HDR SOLD TAIL TO FEM 24	1
454903001	MTG KIT FOR 24-POS"CHAMP"	1
575410007	WASHER FIBER #4 (.250 OD)	2
575470005	WASHER FLAT SIZE #4 NYLON	2
576010001	WASHER SPLIT LOCK SIZE 10	2

PART NUMBER	DESCRIPTION	QUANTITY PER
591003030	WIRE SINGLE BLK AWG 30	1
591503030	WIRE SINGLE GRN AWG 30	1
591603030	WIRE SINGLE BLU AWG 30	1
706010008	ANGLE BRACKET SMALL	2
718901113	PC BD PREASS'Y 8901A-1	1

End of report. 59 Details encountered.


ATN
DAV
NRFD
NDAC
SRQ
EOI
REN
IFC
U52 3448
U50 3448
U34 3448
U35 3448
U47 AC EN
U46 7400
U48 LS04
U42 LS08
U44 LS02
U4 HC14
R1 0n
R2
C20 NOTE 1
C30 NOTE 1
C31 200pF
CR9 IN4448
R11 10K 1/4W
DEL ATN
U26 LS175
U25 LS175
U21 LS133
U14 LS133
U41 LS08
U9 LS133
3A3
UNL
SPED
SPCL
SPE
U29 LS04
U19 LS20
U30 LS10
U31 LS08
U27 8T60
U28 33K
R10 510 1/4W
MLA
MTA
U36 LS27
U43 LS279
U44 LS02
U42 LS08
U43 LS279
U43 9602
R6 5.1K 1/4W
C28 10pF
CAM STR
CAMO
SRQ
U47 LS04
U41 LS08
U33 LS367
U38 LS32
U37 LS08
U46 7400
C21 8pF
U32 LS221
STROBE
RFD
TALK
LISTEN
U51 220
E1
E2
E3
E4
E13
E14
INHIBIT
S1
GP1B ADDRESS
A5
A4
A3
A2
A1
A0
LACS
CLR
P2
LeCroy
RESEARCH SYSTEMS
ELECTRICAL SCHEMATIC
8901A-1
8901A-1-S1
1011

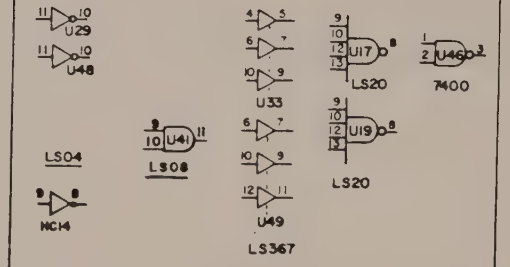

P2
LE
ENABLE
LAM
+5V
U51 220
LS27
LS32
LS10
LS08
LS04
LS02
LS20
LS367
LS133
LS138
LS161
LS221
LS74
LS279
LS804
LS367
9602
U39 LS74
U43 LS279
U41 LS804
U33 LS367
U23 LS138
U24 LS138
U16 LS161
U32 LS221
U11 LS74
U45 9602
U22 LS367
U20 LS367
U15 LS367
U10 LS367
U49 LS367
U47, LS04
U29 LS04
U31, LS08
U47, LS804
U37 LS08
U40 LS10
U49 LS367
U2 2.2K
U3 2.2K
U6 2.2K
U8 LS133
U18 LS133
R4 2.2K 1/4W
R5 5K 1/4W
R3 10K
C22 47pF
C26 0.1
C27 0.1
C32, 56 pF
10K, R12
ETA
XQR
SP1
SP2
SP3
SP4
SPEC
CAMD
SRQ
ATN
DEL ATN
AC ENB
AC EN
DAV
DAT 2
DAT 3
DAT 4
ELR
SPE
SPC
CLR
NOE
RFN
DAC
HC14
P1
P2
8901A-1-SI
2 of 3
1011



NOTES
1. VALUE SELECTED AT TEST

DEVICE	REFERENCE DESIGNATION	+5V	GND
7400	U46	14	7
74LS02	U44	14	7
74LS04	U29,47,48	14	7
74LS08	U31,37,41,42	14	7
74LS10	U30,40	14	7
74HC14	U4	14	7
74LS20	U17,19	14	7
74LS27	U36	14	7
74LS32	U38	14	7
74LS74	U11,39	14	7
74LS133	U8,9,14,18,21	16	7
74LS138	U23,24	16	7
74154	U1,5	24	12
74LS161	U16	16	8
74LS174	U13	16	8
74LS175	U24,26	16	8
74LS221	U32	16	8
74LS279	U43	16	8
74LS367	U10,15,20,22,33 U49	16	8
3448	U34,35,50,52	16	8
8160	U27	16	8
9602	U45	16	8

SPARES



LAST REFERENCE DESIGNATION USED

NOTE: UNLESS OTHERWISE SPECIFIED,
ALL RESISTOR VALUES ARE IN OHMS 1/8W 5%
ALL CAPACITOR VALUES ARE IN MICROFARADS

8901A-1-51

3 of 3

1011

LECROY CORPORATION
8901A-2 PARTS LIST

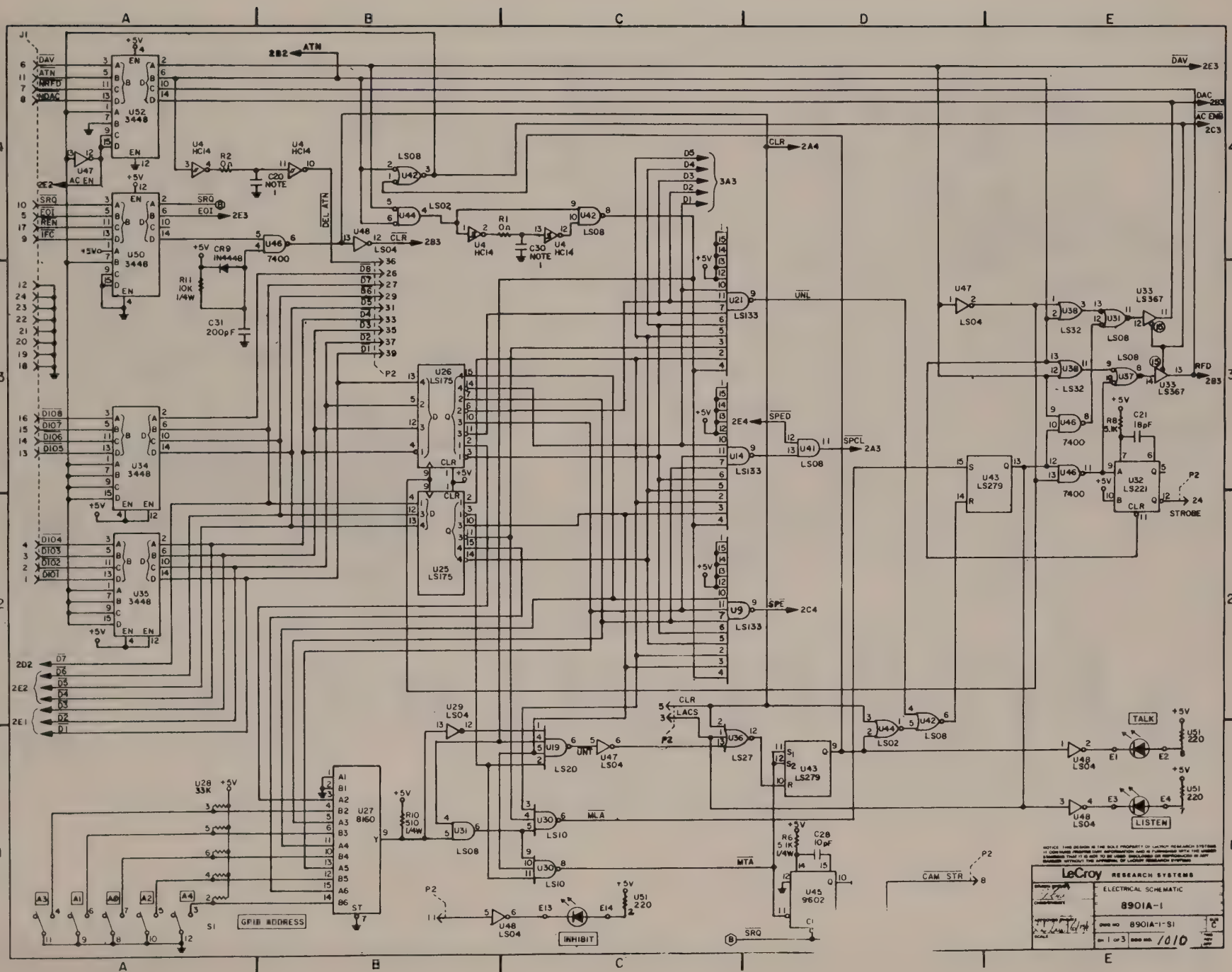
PART NUMBER	DESCRIPTION	QUANTITY PER
103327102	CAP CERA MONO 50V .001 UF	1
103437104	CAP CERA MONO 100V .1 UF	26
142824685	CAP TANT DIP CASE 6.8 UF	1
161030000	RES COMP ZERO OHMS	1
161335103	RES CARBON FILM 10 K	2
161335511	RES CARBON FILM 510 OHMS	2
161335512	RES CARBON FILM 5.1 K	1
161335513	RES CARBON FILM 51 K	1
190122511	RES NETWORK 510 OHMS	5
200031006	IC 2-INPUT AND SN7408N	1
200031028	IC 2-INPUT NAND SN74LS00N	1
200031046	IC HEX INVERTER SN74LS04N	5
200031047	IC 3-INPUT NAND SN74LS10N	2
200031049	IC D-TYP FLOP SN74LS74N	4
200031051	IC 2-INPUT NOR SN74LS02N	3
200031055	IC SHIFT REG SN74LS164N	1
200031073	IC 2-IN POS OR SN74LS32N	2
200031077	IC 3-INPUT AND SN74LS11N	2
200031086	IC 2-INPUT AND SN74LS08N	5
200031100	IC 2-INPUT NAND SN7438N	10
200041001	IC DECODER SN7442N	1
200041033	IC D-TYP FLOP SN74LS174N	1
200041039	IC MONO/MULTIVIB N74LS221	1
200041052	IC 4-BIT REGST DM74LS173N	5
200041057	IC LATCH SN74LS279N	1
200041059	IC BUS DRIVER SN74LS367N	1
200071003	IC 8-BIT REGIST SN74LS374	6
200440161	IC 4-BIT COUNTER S161	1
235010005	DIODE RECTIFIER 1N4005	1
300050001	CHOKE FERRITE SINGLE LEAD	1
309040008	CRYSTAL OSCILLATOR 8 MHZ	1
400900116	PROGRAM PLUG "191" DIP-16	1
403010040	CONN KIT FLAT CABL 40-PIN	2
403181002	HEADER STRT BREAKAW 2-PIN	4
405764007	SOCKET SINGLE WIRE CLOSED	2
433220002	FUSE PICO II 125V 3 AMP	1
454370002	SHUNT 2 POS	2
454710040	HDR RT ANGL MALE/MALE 40	1
592030040	CABLE FLAT AWG 28 40-COND	0
718901123	PC BD PREASS'Y 8901A-2	1

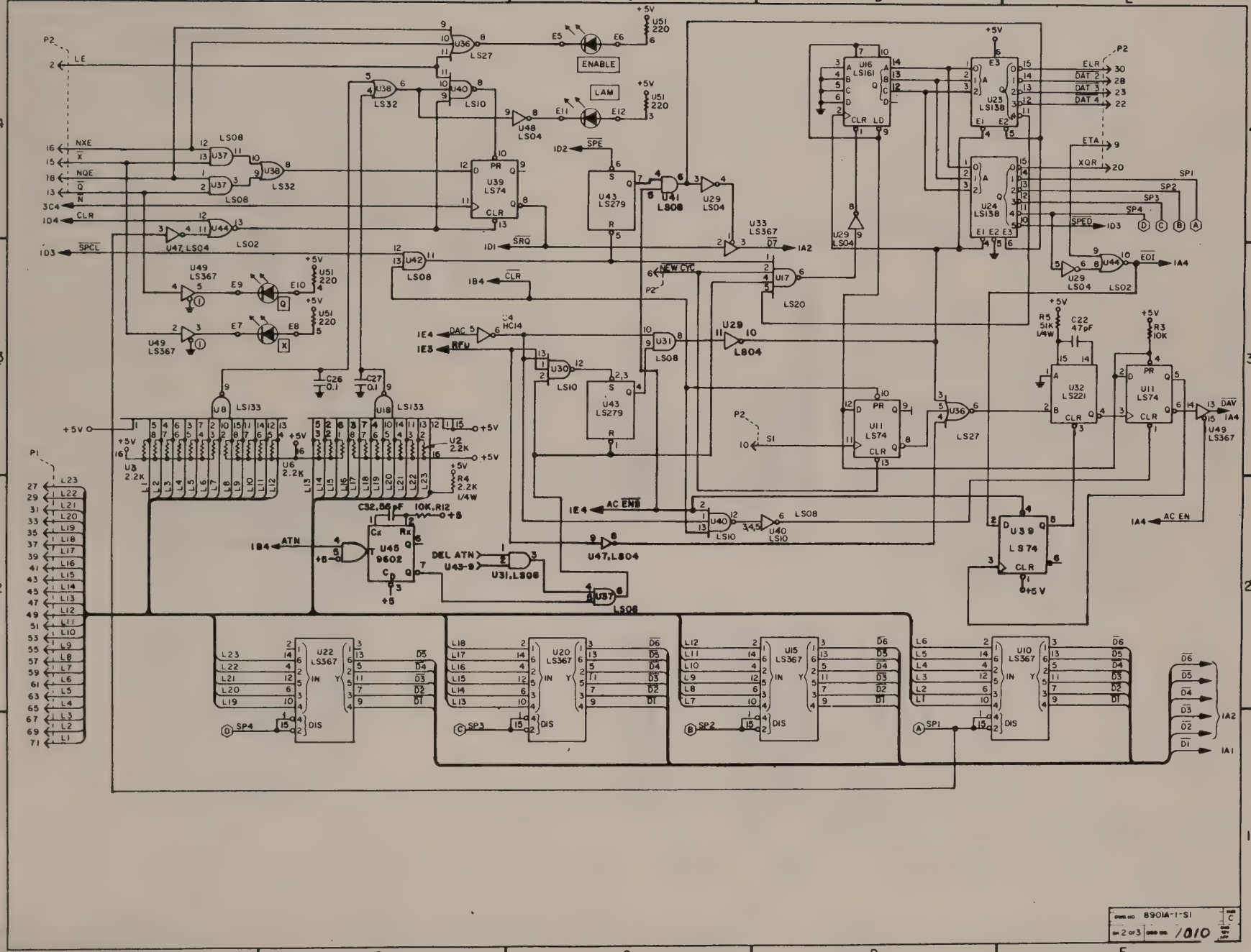
End of report. 40 Details encountered.

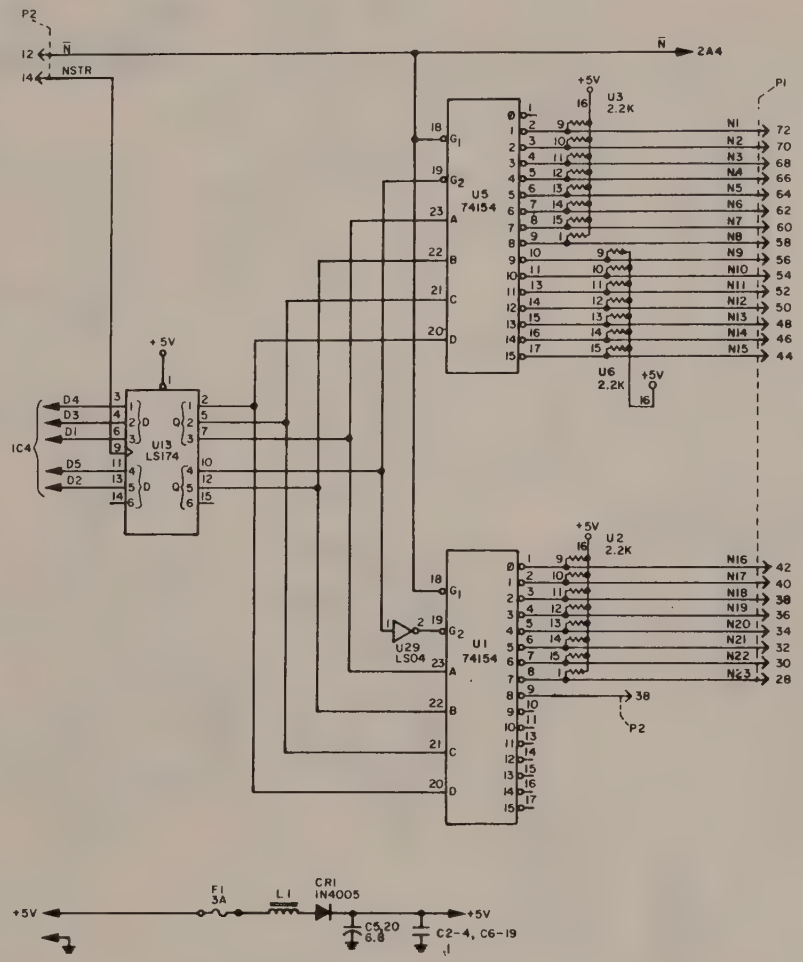
LECROY CORPORATION
8901A-3 PARTS LIST

PART NUMBER	DESCRIPTION	QUANTITY PER
480420201	CABLE GPIB 2 METERS	1
519110002	BUSHING LED BLK MP 52	7
521000004	SPACER HEX 2-56X.417	4
540203001	SIDE COVER CAMAC STD(LIP)	1
540206078	RAIL CAMAC STD TOP W/LIP	2
540206178	RAIL CAMAC STD BOT W/LIP	2
540209102	REAR PANEL CAMAC SIZE 2	1
555430003	CAPTIVE SCREW ASSEMBLY	1
560256005	SCREW PHILIPS 2-56X5/16	4
560440003	SCREW PHILIPS 4-40X3/16	8
560440004	SCREW PHILIPS 4-40X1/4	4
560440005	SCREW PHILIPS 4-40X5/16	4
567440006	SCREW FLAT PHIL 4-40X3/8	4
568256002	SCREW FLAT PHIL 2-56X1/8	4
728901023	FRONT PNL PREASS'Y 8901A	1
738901023	SIDE CAMAC LEFT 8901A	1

End of report. 16 Details encountered.


LeCroy RESEARCH SYSTEMS
ELECTRICAL SCHEMATIC
8901A-1
8901A-1-S1
GPIB ADDRESS
INHIBIT
TALK
LISTEN
STROBE
CAM STR
ATN
DAV
NRFD
NDAC
EOI
REN
IFC
SRQ
DAC
RFD
DEL ATN
UNL
UNT
MLA
MTA
SPE
SPD
LACS
P2
U52 3448
U50 3448
U34 3448
U35 3448
U26 LS175
U25 LS175
U27 8T60
U45 9602
U43 LS279
U32 LS221
U33 LS367
U47 AC EN
C20 NOTE 1
C30 NOTE 1
C31 200pF
C21 18pF
C28 10pF
R1 0Ω
R2 0Ω
R11 10K 1/4W
R10 510 1/4W
R8 5.1K
R6 5.1K 1/4W
CR9 IN4448
S1
1010

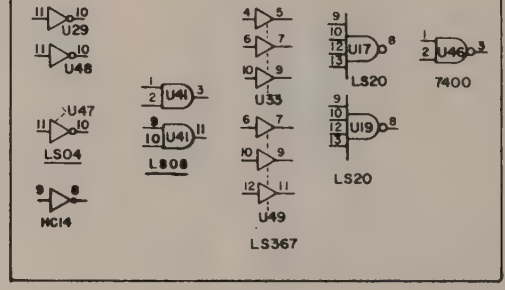

P2
LE
NXE
X
NQE
Q
N
3C4
CLR
ID4
ID3
SPCL
U49 LS367
U51 220
ENABLE
LAM
U48 LS04
U36 LS27
U38 LS32
U40 LS10
U37 LS08
U44 LS02
U47, LS04
U39 LS74
U43 LS279
U41 LS08
U29 LS04
U33 LS367
U42 LS08
U17 LS20
U31 LS08
U30 LS10
U29 L804
U16 LS161
U23 LS138
U24 LS138
E3
ELR
DAT 2
DAT 3
DAT 4
ETA
XQR
SPI
SP2
SP3
SP4
SPED
EOI
U32 LS221
U11 LS74
R5 51K 1/4W
C22 47pF
R3 10K
U49 LS367
U8 LS133
U18 LS133
U3 2.2K
U6 2.2K
U2 2.2K
R4 2.2K 1/4W
C26 0.1
C27 0.1
C32, 56 pF
10K, RI2
U48 9602
DEL ATN
U43-9
U31, LS08
U47, LS04
AC ENB
U40 LS10
U39 LS74
AC EN
U22 LS367
U20 LS367
U15 LS367
U10 LS367
DIS
P1
L23
L22
L21
L20
L19
L18
L17
L16
L15
L14
L13
L12
L11
L10
L9
L8
L7
L6
L5
L4
L3
L2
L1
+5V
+5
8901A-1-SI
2 of 3
1010



NOTES:
1. VALUE SELECTED AT TEST.

DEVICE	REFERENCE DESIGNATION	+5V	GND
7400	U46	14	7
74LS02	U44	14	7
74LS04	U29,47,48	14	7
74LS08	U31,37,41,42	14	7
74LS10	U30,40	14	7
74HC14	U4	14	7
74LS20	U17,19	14	7
74LS27	U36	14	7
74LS32	U38	14	7
74LS74	U11,39	14	7
74LS133	U8,9,14,18,21	16	7
74LS138	U23,24	16	7
74154	U1,5	24	12
74LS161	U16	16	8
74LS174	U13	16	8
74LS175	U24,26	16	8
74LS221	U32	16	8
74LS279	U43	16	8
74LS367	U10,15,20,22,33 U49	16	8
3448	U34,35,50,52	16	8
8160	U27	16	8
9602	U45	16	8

SPARES



LAST REFERENCE DESIGNATION USED

U S... N...

F 7 S 1 F 1 L C 32

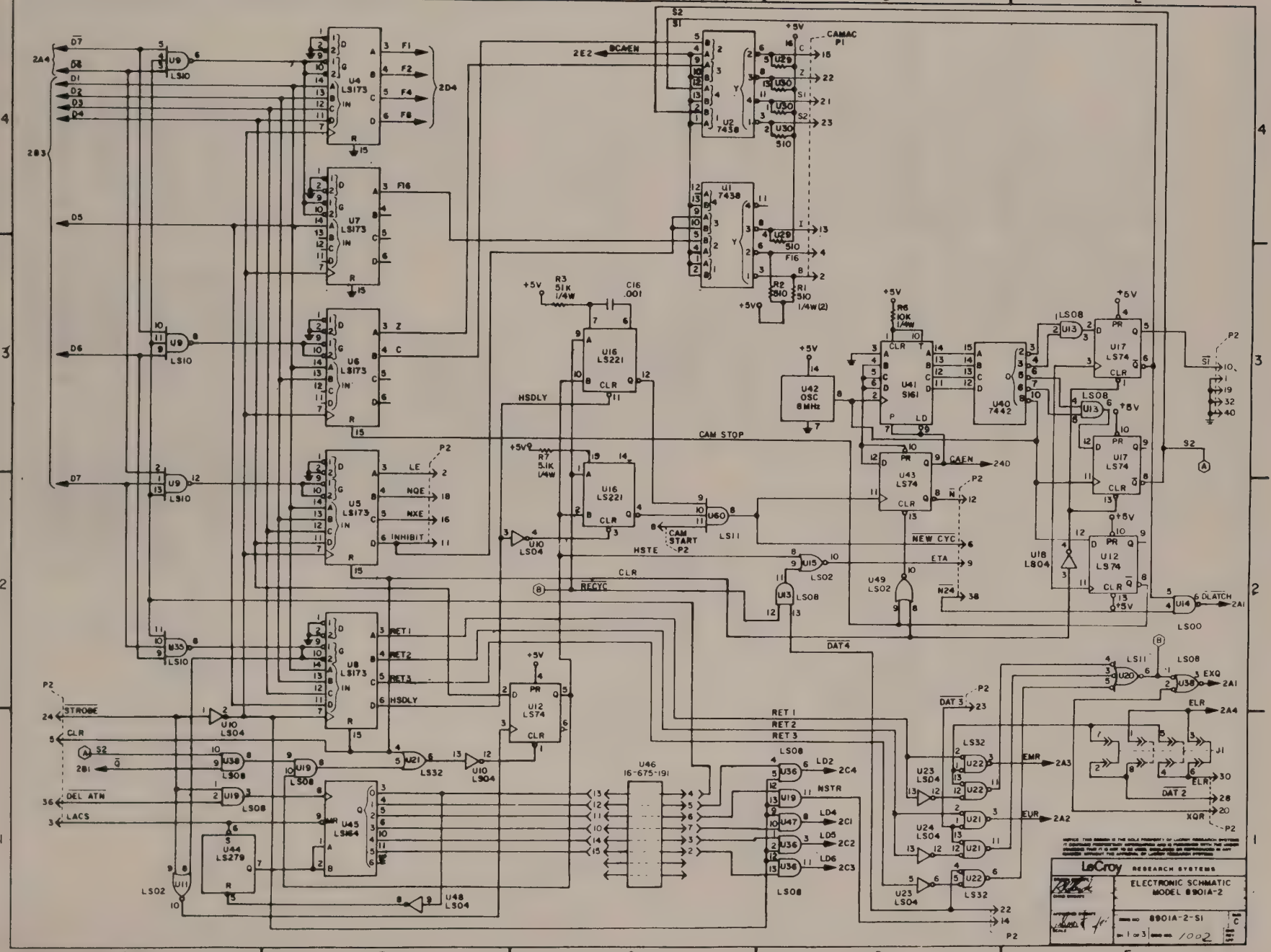
UNLESS OTHERWISE SPECIFIED
*STOR VALUES ARE IN OHMS, 1/8W, 5%
R VALUES ARE IN MICROFARADS

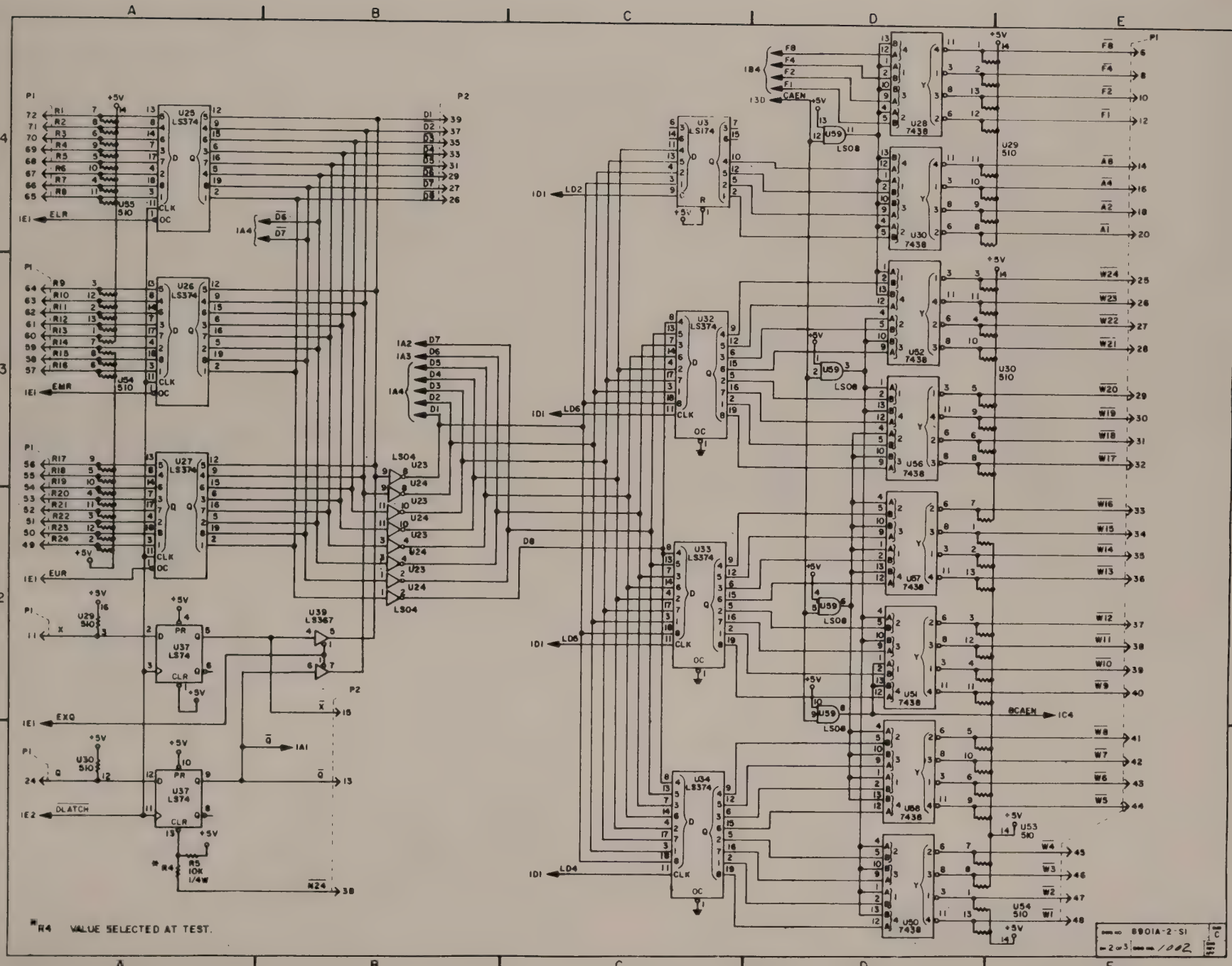
8901A-1-SI

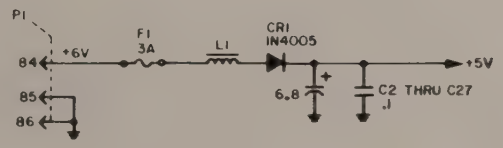
SH 3 OF 3

1010

REV C

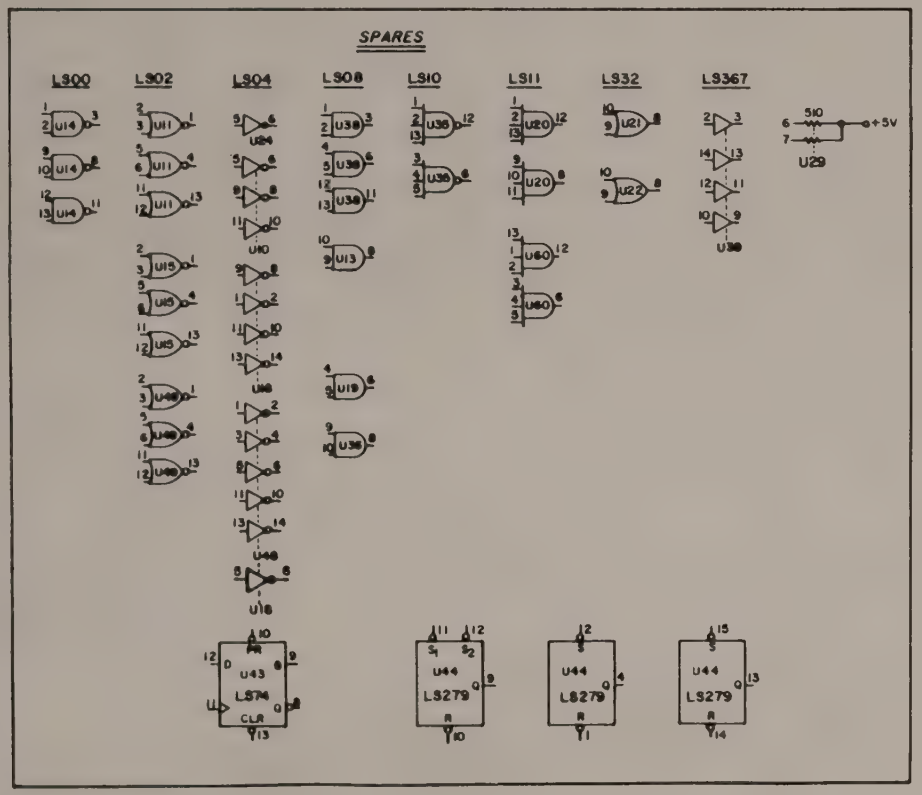

LeCroy RESEARCH SYSTEMS
ELECTRONIC SCHMATIC
MODEL 8901A-2
8901A-2-S1
1002
CAMAC P1
BCAEN
CAM STOP
HSDLY
HSTE
CAM START
NEW CYC
ETA
RECYC
CLR
DAT4
RET 1
RET 2
RET 3
HSDLY
STROBE
DEL ATN
LACS
NSTR
LD2
LD4
LD5
LD6
EMR
EUR
ELR
XQR
DLATCH
U46
16-675-191


A
B
C
D
E
1
2
3
4
P1
P2
+5V
U25 LS374
U26 LS374
U27 LS374
U55 510
U54 510
U29 540
U30 510
U37 LS74
U39 LS367
U23 LS04
U24 LS04
U3 LS174
U32 LS374
U33 LS374
U34 LS374
U28 7438
U30 7438
U52 7438
U56 7438
U57 7438
U51 7438
U58 7438
U50 7438
U59 LS08
U29 510
U30 510
U53 510
U54 510
IE1 ELR
IE1 EMR
IE1 EUR
IE1 EXQ
IE2 DLATCH
IA4
IA2
IA3
IA4
IB4
I3D
IDI LD2
IDI LD6
IDI LD6
IDI LD4
F8
F4
F2
F1
CAEN
BCAEN IC4
D8
R4 VALUE SELECTED AT TEST.
R5 10K 1/4W
8901A-2-SI
2 of 3
1002
C



VOLTAGE AND GROUND PINS CHART

DEVICE	DESIGNATION	+5V	GND
74LS02	U11, 15, 49,	14	7
74LS04	U10, 18, 23, 24, 48	14	7
74LS08	U13, 19, 36, 38, 47	14	7
7408	U59	14	7
74LS10	U9, 35	14	7
74LS11	U20, 60	14	7
74LS32	U21, 22	14	7
7438	U1, 2, 28, 31, 50, 51, 52, 56, 57, 58	14	7
7442	U40	14	7
74LS74	U12, 17, 37, 43	14	7
74S161	U41	16	8
74LS164	U45	16	8
74LS173	U4, 5, 6, 7, 8	16	8
74LS174	U3	16	8
74LS221	U16	16	8
74LS279	U44	16	8
74LS367	U39	16	8
74LS374	U25, 26, 27, 32, 33, 34	20	10
74LS00	U14	14	7



LAST REFERENCE DESIGNATION USED

U40 P2 J1 R67 C27 Y1 K1 F1

NOTE UNLESS OTHERWISE SPECIFIED.
ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%
ALL CAPACITOR VALUES ARE IN MICROFARADS

8901A-2-SI C

SHEET 3 OF 3 1002

0259520

LECROY/8901A

AUTHOR

CAMAC TO GPIB INTERFACE

TITLE

DATE DUE	BORROWER'S NAME
	Tony DiFranco

www.manualsplus.com
1033908